

EL1 69833885

1 RADIO FREQUENCY DATA COMMUNICATIONS DEVICE

2  
3 CROSS REFERENCE TO RELATED APPLICATIONS

4 ~~Sub A~~ This application claims priority from U.S. Provisional Application  
5 60/017,900, filed May 13, 1996, titled "Radio Frequency Data  
6 Communication Device."

7  
8 COPYRIGHT AUTHORIZATION

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15  
16 REFERENCE TO MICROFICHE

17 Appended hereto is a microfiche copy of a software guide entitled  
18 "Micron RFID Systems Developer's Guide," May 2, 1996. This  
19 appendix has 5 microfiche providing 266 total frames.

20  
21 TECHNICAL FIELD

22 This invention relates to radio frequency communication devices.  
23 More particularly, the invention relates to radio frequency identification  
24

1 devices for inventory control, object monitoring, or for determining the  
2 existence, location or movement of objects.

### 3 4 BACKGROUND OF THE INVENTION

5 As large numbers of objects are moved in inventory, product  
6 manufacturing, and merchandising operations, there is a continuous  
7 challenge to accurately monitor the location and flow of objects.  
8 Additionally, there is a continuing goal to interrogate the location of  
9 objects in an inexpensive and streamlined manner. Furthermore, there  
10 is a need for tag devices suitably configured to mount to a variety of  
11 objects including goods, items, persons, or animals, or substantially any  
12 moving or stationary and animate or inanimate object. One way of  
13 tracking objects is with an electronic identification system.

14 One presently available electronic identification system utilizes a  
15 magnetic field modulation system to monitor tag devices. An  
16 interrogator creates a magnetic field that becomes detuned when the tag  
17 device is passed through the magnetic field. In some cases, the tag  
18 device may be provided with a unique identification code in order to  
19 distinguish between a number of different tags. Typically, the tag  
20 devices are entirely passive (have no power supply), which results in a  
21 small and portable package. However, this identification system is only  
22 capable of distinguishing a limited number of tag devices, over a  
23 relatively short range, limited by the size of a magnetic field used to  
24 supply power to the tags and to communicate with the tags.

Another electronic identification system utilizes an RF transponder device affixed to an object to be monitored, in which an interrogator transmits an interrogation signal to the device. The device receives the signal, then generates and transmits a responsive signal. The interrogation signal and the responsive signal are typically radio-frequency (RF) signals produced by an RF transmitter circuit. Since RF signals can be transmitted over greater distances than magnetic fields, RF-based transponder devices tend to be more suitable for applications requiring tracking of a tagged device that may not be in close proximity to an interrogator. For example, RF-based transponder devices tend to be more suitable for inventory control or tracking.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

Preferred embodiments of the invention are described below with reference to the following accompanying drawings. Like names for circuit blocks indicate like components. Where there are a plurality of identical circuit blocks, detailed drawings are provided for one such circuit block. Some circuit schematics have been numbered in a hierarchial manner to reflect the hierarchial nature of these drawings. Notwithstanding the order in which the figures are numbered, note that some detailed drawings provide details to blocks included in more than one higher level drawing. Some circuit schematics have been broken up into many portions due to size requirements for patent drawings.



1 Fig. 1 is a high level circuit schematic showing a circuit  
2 embodying the invention.

3 Fig. 2 is a front view of an employee badge according to but one  
4 embodiment the invention.

5 Fig. 3 is a front view of a radio frequency identification tag  
6 according to another embodiment of the invention.

7 Fig. 4 is a block diagram of an electronic identification system  
8 according to the invention and including an interrogator and the tag of  
9 Fig. 3.

10 Fig. 5 is a high level circuit schematic of a monolithic  
11 semiconductor integrated circuit utilized in the devices of Figs. 1-4.

12 Fig. 6 is a graph illustrating how Figs. 6AA-EK are to be  
13 assembled. After such assembly, Figs. 6AA-EK provide a circuit  
14 drawing of another high level circuit schematic of the monolithic  
15 semiconductor integrated circuit of Fig. 5, showing pads and other  
16 details.

17 Fig. 6.01 is a layout diagram illustrating the physical layout of  
18 various components on an integrated circuit die, in accordance with one  
19 embodiment of the invention. The physical locations and sizes of  
20 components relative to other components are shown. Boundaries  
21 between various blocks may be approximate in the sense that portions  
22 of certain blocks may extend into other blocks.

1 Fig. 7 is a graph illustrating how Figs. 7AA-HJ are to be  
2 assembled. After such assembly, Figs. 7AA-HJ provide a circuit drawing  
3 of a data processor "dataproc" included in the circuit of Figs. 6AA-EK.

4 Fig. 7.01 is a graph illustrating how Figs. 7.01AA-BB are to  
5 be assembled. After such assembly, Figs. 7.01AA-BB provide a circuit  
6 drawing of a processor clock generator "clk" included in the circuit of  
7 Figs. 7AA-HJ.

8 Fig. 7.0101 is a graph illustrating how Figs.  
9 7.0101AA-BB are to be assembled. After such assembly, Figs.  
10 7.0101AA-BB provide a circuit drawing of a processor clock controller  
11 "clkctl" included in the circuit of Figs. 7.01AA-BB.

12 Fig. 7.0102 is a graph illustrating how Figs.  
13 7.0102AE-DJ are to be assembled. After such assembly, Figs.  
14 7.0102AE-DJ provide a circuit drawing of a phase generator "clkph"  
15 included in the circuit of Figs. 7.01AA-BB.

16 Fig. 7.0103 is a graph illustrating how Figs.  
17 7.0103AA-BD are to be assembled. After such assembly, Figs.  
18 7.0103AA-BD provide a circuit drawing of a state generator "clkst"  
19 included in the circuit of Figs. 7.01AA-BB.

20 Fig. 7.010301 is a graph illustrating how Figs.  
21 7.010301AA-BB are to be assembled. After such assembly, Figs.  
22 7.010301AA-BB provide a circuit drawing of a clock generator counter  
23 bit "clkebit" included in the circuit of Figs. 7.0103AA-BD.  
24

Fig. 7.02 is a graph illustrating how Figs. 7.02AA-BF are to be assembled. After such assembly, Figs. 7.02AA-BF provide a circuit drawing of an address decoder "adrdec" included in the circuit of Figs. 7AA-BF.

Fig. 7.03 is a graph illustrating how Figs. 7.03AA-EH are to be assembled. After such assembly, Figs. 7.03AA-EH provide a circuit drawing of a 512 byte RAM "ram" included in the circuit of Figs. 7AA-HJ.

Fig. 7.0301 is a graph illustrating how Figs. 7.0301AA-BB are to be assembled. After such assembly, Figs. 7.0301AA-BB provide a circuit drawing of a RAM control circuit "ramctl" included in the circuit of Figs. 7.03AA-BB.

Fig. 7.0302 is a graph illustrating how Figs. 7.0302AA-AC are to be assembled. After such assembly, Figs. 7.0302AA-AC provide a circuit drawing of an 8x4 RAM array "ram8x4" included in the circuit of Figs. 7.03AA-EH.

Fig. 7.030201 is a circuit drawing of a six transistor RAM cell "ramcell" included in the circuit of Figs. 7.0302AA-AC.

Fig. 7.0303 is a graph illustrating how Figs. 7.0303AA-AD are to be assembled. After such assembly, Figs. 7.0303AA-AD provide a circuit drawing of a RAM precharge circuit "rampch" included in the circuit of Figs. 7.03AA-EH.

Fig. 7.0304 is a graph illustrating how Figs. 7.0304AA-AD are to be assembled. After such assembly, Figs. 7.0304AA-AD provide a circuit drawing of a second RAM precharge circuit "ramdch" included in the circuit of Figs. 7.03AA-EH.

Fig. 7.0305 is a circuit drawing of a RAM address buffer "ramadb" included in the circuit of Figs. 7.03AA-EH.

Fig. 7.0306 is a graph illustrating how Figs. 7.0306AA-BA are to be assembled. After such assembly, Figs. 7.0306AA-BA provide a circuit drawing of a RAM word line driver "ramwdr" included in the circuit of Figs. 7.03AA-EH.

Fig. 7.0307 is a graph illustrating how Figs. 7.0307AA-BB are to be assembled. After such assembly, Figs. 7.0307AA-BB provide a circuit drawing of a RAM word line decoder "ramwdec" included in the circuit of Figs. 7.03AA-EH.

Fig. 7.0308 is a graph illustrating how Figs. 7.0308AA-BB are to be assembled. After such assembly, Figs. 7.0308AA-BB provide a circuit drawing of a RAM column select decode circuit "ramcdec" included in the circuit of Figs. 7.03AA-EH.

Fig. 7.0309 is a graph illustrating how Figs. 7.0309AA-BG are to be assembled. After such assembly, Figs. 7.0309AA-BG provide a circuit drawing of a RAM column selector "ramcsel" included in the circuit of Figs. 7.03AA-EH.

Fig. 7.0310 is a graph illustrating how Figs. 7.0310AA-BB are to be assembled. After such assembly, Figs.

1 7.0310AA-BB provide a circuit drawing of a RAM databus interface  
2 "ramdb" included in the circuit of Figs. 7.03AA-EH.

3 Fig. 7.04 is a graph illustrating how Figs. 7.04AA-HJ are to  
4 be assembled. After such assembly, Figs. 7.04AA-HJ provide a circuit  
5 drawing of a ROM "rom" included in the circuit of Figs. 7AA-HJ.

6 Fig. 7.0401 is a graph illustrating how Figs.  
7 7.0401AA-BB are to be assembled. After such assembly, Figs.  
8 7.0401AA-BB provide a circuit drawing of a ROM control logic circuit  
9 "romctl" included in the circuit of Figs. 7.04AA-HJ.

10 Fig. 7.0402 is a graph illustrating how Figs.  
11 7.0402AA-AB are to be assembled. After such assembly, Figs.  
12 7.0402AA-AB provide a circuit drawing of a ROM bit line precharge  
13 circuit "rompch" included in the circuit of Figs. 7.04AA-HJ.

14 Fig. 7.0403 is a graph illustrating how Figs.  
15 7.0403AA-BB are to be assembled. After such assembly, Figs.  
16 7.0403AA-BB provide a circuit drawing of a ROM word line driver  
17 "romwdr" included in the circuit of Figs. 7.04AA-HJ.

18 Fig. 7.0404 is a graph illustrating how Figs.  
19 7.0404AB-DC are to be assembled. After such assembly, Figs.  
20 7.0404AA-DC provide a circuit drawing of a ROM word block decoder  
21 "romwdec\_rev" included in the circuit of Figs. 7.04AA-HJ.

22 Fig. 7.0405 is a graph illustrating how Figs.  
23 7.0405AA-BA are to be assembled. After such assembly, Figs.

FIG. 7.0405AA-BA

7.0405AA-BA provide a circuit drawing of a ROM bit line address driver "romblldr" included in the circuit of Figs. 7.04AA-HJ.

Fig. 7.0406 is a graph illustrating how Figs. 7.0406AA-CK are to be assembled. After such assembly, Figs. 7.0406AA-CK provide a circuit drawing of a ROM bit line decoder "rombldec" included in the circuit of Figs. 7.04AA-HJ.

Fig. 7.0407 is a graph illustrating how Figs. 7.0407AA-AB are to be assembled. After such assembly, Figs. 7.0407AA-AB provide a circuit drawing of a ROM sense amplifier "romsns" included in the circuit of Figs. 7.04AA-HJ.

Fig. 7.05 is a graph illustrating how Figs. 7.05AA-CB are to be assembled. After such assembly, Figs. 7.05AA-CB provide a circuit drawing of an instruction register "insreg" included in the circuit of Figs. 7AA-HJ.

Fig. 7.0501 is a graph illustrating how Figs. 7.0501AA-AB are to be assembled. After such assembly, Figs. 7.0501AA-AB provide a circuit drawing of an instruction register cell "insrcel" included in the circuit of Figs. 7.05AA-CB.

Fig. 7.06 is a graph illustrating how Figs. 7.06AA-CN are to be assembled. After such assembly, Figs. 7.06AA-CN provide a circuit drawing of an instruction decoder PLA "insdec" included in the circuit of Figs. 7AA-HJ.

Fig. 7.0601 is a graph illustrating how Figs. 7.0601AA-HI are to be assembled. After such assembly, Figs.

1 7.0601AA-HI provide a circuit drawing of an instruction decoder  
2 "insdec1" included in the circuit of Figs. 7AA-HJ.

3 Fig. 7.0602 is a graph illustrating how Figs.  
4 7.0602AA-JH are to be assembled. After such assembly, Figs.  
5 7.0602AA-JH provide a circuit drawing of an instruction decoder (second  
6 section) "insdec2" included in the circuit of Figs. 7AA-HJ.

7 Fig. 7.0603 is a graph illustrating how Figs.  
8 7.0603AA-JI are to be assembled. After such assembly, Figs.  
9 7.0603AA-JI provide a circuit drawing of an instruction decoder (third  
10 section) "insdec3" included in the circuit of Figs. 7AA-HJ.

11 Fig. 7.0604 is a graph illustrating how Figs.  
12 7.0604AA-JI are to be assembled. After such assembly, Figs.  
13 7.0604AA-JI provide a circuit drawing of an instruction decoder (fourth  
14 section) "insdec4" included in the circuit of Figs. 7AA-HJ.

15 Fig. 7.060401 is a circuit drawing of an  
16 instruction decoder ROM amp "insramp" included in the circuit of  
17 Figs. 7.0604AA-JI.

18 Fig. 7.060402 is a circuit drawing of an  
19 instruction decoder PLA amp "inspamp" included in the circuit of  
20 Figs. 7.0604AA-JI.

21 Fig. 7.060403 is a circuit drawing of an  
22 instruction decoder PLA latch "insplat" included in the circuit of  
23 Figs. 7.0604AA-JI.  
24

1 Fig. 7.07 is a graph illustrating how Figs. 7.07AA-BB are to  
2 be assembled. After such assembly, Figs. 7.07AA-BB provide a circuit  
3 drawing of a conditional qualifier decoder "cqualdec" included in the  
4 circuit of Figs. 7AA-HJ.

5 Fig. 7.08 is a graph illustrating how Figs. 7.08AA-CA are  
6 to be assembled. After such assembly, Figs. 7.08AA-CA provide a  
7 circuit drawing of a databus latch/precharge circuit "dblatch" included in  
8 the circuit of Figs. 7AA-HJ.

9 Fig. 7.09 is a graph illustrating how Figs. 7.09AA-BF are to  
10 be assembled. After such assembly, Figs. 7.09AA-BF provide a circuit  
11 drawing of an arithmetic logic unit "alu" included in the circuit of  
12 Figs. 7AA-HJ.

13 Fig. 7.0901 is a graph illustrating how Figs.  
14 7.0901AA-CE are to be assembled. After such assembly, Figs.  
15 7.0901AA-CE provide a circuit drawing of an ALU low byte "alubyt1"  
16 included in the circuit of Figs. 7.09AA-BF.

17 Fig. 7.090101 is a graph illustrating how Figs.  
18 7.090101AA-AD are to be assembled. After such assembly, Figs.  
19 7.090101AA-AD provide a circuit drawing of a bit "alubit1" included in  
20 the circuit of Figs. 7.0901AA-CE.

21 Fig. 7.09010101 is a circuit drawing of an  
22 ALU bit decoder cell "alubdec" included in the circuit of  
23 Figs. 7.090101AA-AD.  
24



1 Fig. 7.09010102 is a circuit drawing of an  
2 ALU B register cell "alubcell" included in the circuit of  
3 Figs. 7.090101AA-AD.

4 Fig. 7.09010103 is a graph illustrating how  
5 Figs. 7.09010103AA-AB are to be assembled. After such assembly, Figs.  
6 7.09010103AA-AB provide a circuit drawing of an ALU A register cell  
7 "aluacell" included in the circuit of Figs. 7.090101AA-AD.

8 Fig. 7.09010104 is a graph illustrating how  
9 Figs. 7.09010104AA-AB are to be assembled. After such assembly, Figs.  
10 7.09010104AA-AB provide a circuit drawing of an ALU register cell  
11 "alupc" included in the circuit of Figs. 7.090101AA-AD.

12 Fig. 7.09010105 is a circuit drawing of an  
13 ALU register cell "alurcell" included in the circuit of Figs. 7.090101AA-  
14 AD. Such register cells are used for a stack pointer and data pointer.

15 Fig. 7.09010106 is a graph illustrating how  
16 Figs. 7.09010106AA-AB are to be assembled. After such assembly, Figs.  
17 7.09010106AA-AB provide a circuit drawing of an ALU memory address  
18 register "alumar" included in the circuit of Figs. 7.090101AA-AD.

19 Fig. 7.09010107 is a circuit drawing of an  
20 ALU slave cell "aluslave" included in the circuit of Figs. 7.090101AA-  
21 AD.

22 Fig. 7.09010108 is a graph illustrating how  
23 Figs. 7.09010108AA-BC are to be assembled. After such assembly, Figs.  
24

1 7.09010108AA-BC provide a circuit drawing of an ALU adder "aluadd"  
2 included in the circuit of Figs. 7.090101AA-AD.

3 Fig. 7.0902 is a graph illustrating how Figs.  
4 7.0902AA-BD are to be assembled. After such assembly, Figs.  
5 7.0902AA-BD provide a circuit drawing of an ALU high byte "alubyth"  
6 included in the circuit of Figs. 7.09AA-BF.

7 Fig. 7.090201 is a graph illustrating how Figs.  
8 7.090201AA-AC are to be assembled. After such assembly, Figs.  
9 7.090201AA-AC provide a circuit drawing of a bit "alubith" included in  
10 the circuit of Figs. 7.09AA-BF.

11 Fig. 7.10 is a graph illustrating how Figs. 7.10AA-CC are  
12 to be assembled. After such assembly, Figs. 7.10AA-CC provide a  
13 circuit drawing of a timed lockout divider "tld" included in the circuit  
14 of Figs. 7AA-HJ.

15 Fig. 7.1001 is a circuit drawing of a timed lockout  
16 divider cell "tldcel" included in the circuit of Figs. 7.10AA-CC.

17 Fig. 7.11 is a graph illustrating how Figs. 7.11AA-AB are  
18 to be assembled. After such assembly, Figs. 7.11AA-AB provide a  
19 circuit drawing of a timed lockout register "tlorege" included in the  
20 circuit of Figs. 7AA-HJ.

21 Fig. 7.1101 is a graph illustrating how Figs.  
22 7.1101AA-AC are to be assembled. After such assembly, Figs.  
23 7.1101AA-AC provide a circuit drawing of a timed lockout register cell  
24 "tlorcel" included in the circuit of Figs. 7.11AA-AB.

1 Fig. 7.12 is a graph illustrating how Figs. 7.12AA-AC are  
2 to be assembled. After such assembly, Figs. 7.12AA-AC provide a  
3 circuit drawing of a R/W control register "oreg" included in the circuit  
4 of Figs. 7AA-HJ.

5 Fig. 7.1201 is a circuit drawing of a R/W control  
6 register cell "regcell" included in the circuit of Figs. 7.12AA-AC.

7 Fig. 7.13 is a graph illustrating how Figs. 7.13AA-BA are  
8 to be assembled. After such assembly, Figs. 7.13AA-BA provide a  
9 circuit drawing of a status register "sreg" included in the circuit of  
10 Figs. 7AA-HJ.

11 Fig. 7.1301 is a circuit drawing of a status register  
12 cell "sregcel" included in the circuit of Figs. 7.13AA-BA.

13 Fig. 7.14 is a graph illustrating how Figs. 7.14AA-AB are  
14 to be assembled. After such assembly, Figs. 7.14AA-AB provide a  
15 circuit drawing of a serial input/output block "sio" included in the circuit  
16 of Figs. 7AA-HJ.

17 Fig. 7.1401 is a graph illustrating how Figs. 7.1401AA-  
18 GF are to be assembled. After such assembly, Figs. 7.1401AA-GF  
19 provide a circuit drawing of a serial input/output data path "siodata"  
20 included in the circuit of Figs. 7.14AA-AB.

21 Fig. 7.140101 is a graph illustrating how Figs.  
22 7.140101AA-AB are to be assembled. After such assembly, Figs.  
23 7.140101AA-AB provide a circuit drawing of a serial input/output register  
24 cell "sioreg" included in the circuit of Figs. 7.1401AA-AB.

1 Fig. 7.140102 is a circuit drawing of a serial  
2 input/output XOR circuit "sioxor" included in the circuit of  
3 Figs. 7.1401AA-GF.

4 Fig. 7.140103 is a graph illustrating how Figs.  
5 7.140103AA-AB are to be assembled. After such assembly, Figs.  
6 7.140103AA-AB provide a circuit drawing of a bidirectional latch  
7 "siobdlat\_inv" included in the circuit of Figs. 7.1401AA-GF.

8 Fig. 7.140104 is a graph illustrating how Figs.  
9 7.140104AA-AB are to be assembled. After such assembly, Figs.  
10 7.140104AA-AB provide a circuit drawing of a shift register "sioshr"  
11 included in the circuit of Figs. 7.1401AA-GF.

12 Fig. 7.140105 is a graph illustrating how Figs.  
13 7.140105AA-AB are to be assembled. After such assembly, Figs.  
14 7.140105AA-AB provide a circuit drawing of a bidirectional latch  
15 "siobdlat" included in the circuit of Figs. 7.1401AA-GF.

16 Fig. 7.1402 is a graph illustrating how Figs. 7.1402BA-  
17 EI are to be assembled. After such assembly, Figs. 7.1402BA-EI  
18 provide a circuit drawing of serial input/output control logic "sioc1"  
19 included in the circuit of Figs. 7.14AA-AB.

20 Fig. 7.140201 is a graph illustrating how Figs.  
21 7.140201AA-BB are to be assembled. After such assembly, Figs.  
22 7.140201AA-BB provide a circuit drawing of a counter bit "siocbit"  
23 included in the circuit of Figs. 7.1402AA-AB  
24

Fig. 7.15 is a graph illustrating how Figs. 7.15AA-EC are to be assembled. After such assembly, Figs. 7.15AA-EC provide a circuit drawing of a data interleaver (which interleaves two thirteen bit words) "dil" included in the circuit of Figs. 7AA-HJ.

Fig. 7.1501 is a graph illustrating how Figs. 7.1501AA-CA are to be assembled. After such assembly, Figs. 7.1501AA-CA provide a circuit drawing of a data interleaver shift register "dil\_sreg" included in the circuit of Figs. 7.15AA-EC.

Fig. 7.1502 is a graph illustrating how Figs. 7.1502AA-CA are to be assembled. After such assembly, Figs. 7.1502AA-CA provide a circuit drawing of a data interleaver shift register with parallel load "dil\_plsreg" included in the circuit of Figs. 7.15AA-EC.

Fig. 7.150201 is a circuit drawing of a data interleaver shift register bit "dil\_sregbit" included in the circuit of Figs. 7.1502AA-CA.

Fig. 7.16 is a graph illustrating how Figs. 7.16AA-CD are to be assembled. After such assembly, Figs. 7.16AA-CD provide a circuit drawing of a convolutional encoder and preamble generator "conv" included in the circuit of Figs. 7AA-HJ.

Fig. 7.1601 is a circuit drawing of a shift register cell "convshr" included in the circuit of Figs. 7.16AA-CD.

Fig. 7.1602 is a circuit drawing of a summer "convsum" included in the circuit of Figs. 7.16AA-CD.

Fig. 7.17 is a graph illustrating how Figs. 7.17AA-BB are to be assembled. After such assembly, Figs. 7.17AA-BB provide a circuit drawing of a shift register input data MUX "shdcel" included in the circuit of Figs. 7AA-HJ.

Fig. 7.18 is a graph illustrating how Figs. 7.18AA-CC are to be assembled. After such assembly, Figs. 7.18AA-CC provide a circuit drawing of a digital port output controller "doutport" included in the circuit of Figs. 7AA-HJ.

Fig. 8 is a graph illustrating how Figs. 8AA-CB are to be assembled. After such assembly, Figs. 8AA-CB provide a circuit drawing of an RF processor "rfproc" included in the circuit of Figs. 6AA-EK.

Fig. 8.01 is a graph illustrating how Figs. 8.01AA-DE are to be assembled. After such assembly, Figs. 8.01AA-DE provide a circuit drawing of a receiver "rx" included in the circuit of Figs. 8AA-CB.

Fig. 8.0101 is a graph illustrating how Figs. 8.0101AA-CB are to be assembled. After such assembly, Figs. 8.0101AA-CB provide a circuit drawing of a Schottky diode detector "diodedet" included in the circuit of Figs. 8.01AA-DE.

Fig. 8.0102 is a graph illustrating how Figs. 8.0102AA-BD are to be assembled. After such assembly, Figs. 8.0102AA-BD provide a circuit drawing of a CMOS square law detector "cmosdet" included in the circuit of Figs. 8.01AA-DE.

1 Fig. 8.0103 is a graph illustrating how Figs.  
2 8.0103AA-CF are to be assembled. After such assembly, Figs.  
3 8.0103AA-CF provide a circuit drawing of a video amplifier "videoamp1"  
4 included in the circuit of Figs. 8.01AA-DE.

5 Fig. 8.0104 is a graph illustrating how Figs.  
6 8.0104AA-BC are to be assembled. After such assembly, Figs.  
7 8.0104AA-BC provide a circuit drawing of a second video amplifier  
8 "videoamp2" included in the circuit of Figs. 8.01AA-DE.

9 Fig. 8.0105 is a graph illustrating how Figs.  
10 8.0105AA-ED are to be assembled. After such assembly, Figs.  
11 8.0105AA-ED provide a circuit drawing of a comparator "comparator"  
12 included in the circuit of Figs. 8.01AA-DE.

13 Fig. 8.0106 is a graph illustrating how Figs.  
14 8.0106AA-CD are to be assembled. After such assembly, Figs.  
15 8.0106AA-CD provide a circuit drawing of an RF detect circuit "rxdet"  
16 included in the circuit of Figs. 8.01AA-DE.

17 Fig. 8.0107 is a graph illustrating how Figs.  
18 8.0107AA-GN are to be assembled. After such assembly, Figs.  
19 8.0107AA-GN provide a circuit drawing of a receiver bias generator  
20 "rxbias" included in the circuit of Figs. 8.01AA-DE.

21 Fig. 8.0108 is a graph illustrating how Figs.  
22 8.0108AA-AC are to be assembled. After such assembly, Figs.  
23 8.0108AA-AC provide a circuit drawing of a data transition detector  
24 "datatx" included in the circuit of Figs. 8.01AA-DE.

Fig. 8.02 is a graph illustrating how Figs. 8.02AA-BC are to be assembled. After such assembly, Figs. 8.02A-BC provide a circuit drawing of a low power frequency locked loop "lpfl" included in the circuit of Figs. 8AA-CB.

Fig. 8.0201 is a graph illustrating how Figs. 8.0201AA-AB are to be assembled. After such assembly, Figs. 8.0201AA-AB provide a circuit drawing of a timed lockout divider cell "tldcel\_bypass" included in the circuit of Figs. 8.02AA-BC.

Fig. 8.0202 is a graph illustrating how Figs. 8.0202AA-CD are to be assembled. After such assembly, Figs. 8.0202AA-CD provide a circuit drawing of a low power frequency locked loop frequency comparator "freqcomp" included in the circuit of Figs. 8.02AA-BC.

Fig. 8.0203 is a graph illustrating how Figs. 8.0203AA-BC are to be assembled. After such assembly, Figs. 8.0203AA-BC provide a circuit drawing of an up/down counter "udcounter" included in the circuit of Figs. 8.02AA-BC.

Fig. 8.020301 is a graph illustrating how Figs. 8.020301AA-BB are to be assembled. After such assembly, Figs. 8.020301AA-BB provide a circuit drawing of an adder "udcounter\_adder" included in the circuit of Figs. 8.0203AA-BC.

Fig. 8.020302 is a graph illustrating how Figs. 8.020302AA-AB are to be assembled. After such assembly, Figs.



8.020302AA-AB provide a circuit drawing of a D type flip-flop "udcounter\_dff" included in the circuit of Figs. 8.0203AA-BC.

Fig. 8.0204 is a graph illustrating how Figs. 8.0204AA-EJ are to be assembled. After such assembly, Figs. 8.0204AA-EJ provide a circuit drawing of a low power current controlled oscillator "lpcco" included in the circuit of Figs. 8.02AA-BC.

Fig. 8.0205 is a circuit drawing of a timed lockout divider cell "tldcel" included in the circuit of Figs. 8.02AA-BC.

Fig. 8.03 is a graph illustrating how Figs. 8.03AA-AB are to be assembled. After such assembly, Figs. 8.03AA-AB provide a circuit drawing of a counter bit "lpfl\_cbit" included in the circuit of Figs. 8AA-CB.

Fig. 8.04 is a graph illustrating how Figs. 8.04AA-EE are to be assembled. After such assembly, Figs. 8.04AA-EE provide a circuit drawing of a receiver wake up controller "rxwu" included in the circuit of Figs. 8AA-CB.

Fig. 8.0401 is a graph illustrating how Figs. 8.0401AA-AB are to be assembled. After such assembly, Figs. 8.0401AA-AB provide a circuit drawing of wake up abort logic "wuabort" included in the circuit of Figs. 8.04AA-EE.

Fig. 8.040101 is a graph illustrating how Figs. 8.040101AA-AB are to be assembled. After such assembly, Figs. 8.040101AA-AB provide a circuit drawing of wake up abort logic counter bit "wuabort\_cbit" included in the circuit of Figs. 8.0401AA-AB.

1 Fig. 8.0402 is a graph illustrating how Figs.  
2 8.0402AA-AB are to be assembled. After such assembly, Figs.  
3 8.0402AA-AB provide a circuit drawing of a timed lockout divider cell  
4 "tldcel" included in the circuit of Figs. 8.04AA-EE.

5 Fig. 8.05 is a graph illustrating how Figs. 8.05AA-DE are  
6 to be assembled. After such assembly, Figs. 8.05AA-DE provide a  
7 circuit drawing of a digital clock and data recovery circuit "dcr" included  
8 in the circuit of Figs. 8AA-CB.

9 Fig. 8.0501 is a graph illustrating how Figs.  
10 8.0501AA-BE are to be assembled. After such assembly, Figs.  
11 8.0501AA-BE provide a circuit drawing of a PLL start-up circuit  
12 "dcr\_startup" included in the circuit of Figs. 8.05AA-DE.

13 Fig. 8.050101 is a graph illustrating how Figs.  
14 8.050101AA-AB are to be assembled. After such assembly, Figs.  
15 8.050101AA-AB provide a circuit drawing of a shift register cell  
16 "dcr\_sreg" included in the circuit of Figs. 8.0501AA-BE.

17 Fig. 8.050102 is a graph illustrating how Figs.  
18 8.050102AA-AB are to be assembled. After such assembly, Figs.  
19 8.050102AA-AB provide a circuit drawing of a counter bit  
20 "dcr\_counterbit" included in the circuit of Figs. 8.0501AA-BE.

21 Fig. 8.0502 is a graph illustrating how Figs.  
22 8.0502AA-CD are to be assembled. After such assembly, Figs.  
23 8.0502AA-CD provide a circuit drawing of a PLL state machine  
24 "dcr\_statemachine" included in the circuit of Figs. 8.05AA-DE.

1 Fig. 8.0503 is a graph illustrating how Figs.  
2 8.0503AA-FN are to be assembled. After such assembly, Figs.  
3 8.0503AA-FN provide a circuit drawing of a DCR bias generator  
4 "dcr\_bias" included in the circuit of Figs. 8.05AA-DE.

5 Fig. 8.0504 is a graph illustrating how Figs.  
6 8.0504AA-EE are to be assembled. After such assembly, Figs.  
7 8.0504AA-EE provide a circuit drawing of a VCO control voltage  
8 generator "dcr\_vcocontrol" included in the circuit of Figs. 8.05AA-DE.

9 Fig. 8.050401 is a graph illustrating how Figs.  
10 8.050401AA-CK are to be assembled. After such assembly, Figs.  
11 8.050401AA-CK provide a circuit drawing of a coarse step generator  
12 "dcr\_coarsestepgen" included in the circuit of Figs. 8.0504AA-EE.

13 Fig. 8.050402 is a graph illustrating how Figs.  
14 8.050402AA-CJ are to be assembled. After such assembly, Figs.  
15 8.050402AA-CJ provide a circuit drawing of a medium step generator  
16 "dcr\_medstepgen" included in the circuit of Figs. 8.0504AA-EE.

17 Fig. 8.050403 is a graph illustrating how Figs.  
18 8.050403AA-BI are to be assembled. After such assembly, Figs.  
19 8.050403AA-BI provide a circuit drawing of a medium fine step  
20 generator "dcr\_medfinestepgen" included in the circuit of  
21 Figs. 8.0504AA-EE.

22 Fig. 8.050404 is a graph illustrating how Figs.  
23 8.050404AA-BB are to be assembled. After such assembly, Figs.  
24

1 8.050404AA-BB provide a circuit drawing of a fine step controller  
2 "dcr\_finestepctrl" included in the circuit of Figs. 8.0504AA-EE.

3 Fig. 8.050405 is a graph illustrating how Figs.  
4 8.050405AA-EJ are to be assembled. After such assembly, Figs.  
5 8.050405AA-EJ provide a circuit drawing of a fine step generator  
6 "dcr\_finestepgen" included in the circuit of Figs. 8.0504AA-EE.

7 Fig. 8.0505 is a graph illustrating how Figs.  
8 8.0505AA-EF are to be assembled. After such assembly, Figs.  
9 8.0505AA-EF provide a circuit drawing of a receiver VCO "dcr\_vco"  
10 included in the circuit of Figs. 8.05AA-DE.

11 Fig. 8.0506 is a graph illustrating how Figs.  
12 8.0506AA-BB are to be assembled. After such assembly, Figs.  
13 8.0506AA-BB provide a circuit drawing of an RX clock generator  
14 "dcr\_rxclkgen" included in the circuit of Figs. 8.05AA-DE.

15 Fig. 8.050601 is a circuit drawing of an RX  
16 clock generator flip-flop "dcr\_rxclkgenff" included in the circuit of  
17 Figs. 8.0506AA-BB.

18 Fig. 8.0507 is a graph illustrating how Figs.  
19 8.0507AA-AB are to be assembled. After such assembly, Figs.  
20 8.0507AA-AB provide a circuit drawing of a PLL non-overlapping clock  
21 generator "dcr\_clkgen" included in the circuit of Figs. 8.05AA-DE.

22 Fig. 8.06 is a graph illustrating how Figs. 8.06AA-ED are  
23 to be assembled. After such assembly, Figs. 8.06AA-ED provide a  
24

1 circuit drawing of a BPSK/AM/Backscatter transmitter "tx" included in  
2 the circuit of Figs. 8AA-CB.

3 Fig. 8.0601 is a graph illustrating how Figs.  
4 8.0601AA-BB are to be assembled. After such assembly, Figs.  
5 8.0601AA-BB provide a circuit drawing of a transmitter PLL "txpllfsyn"  
6 included in the circuit of Figs. 8.06AA-ED.

7 Fig. 8.060101 is a graph illustrating how Figs.  
8 8.060101AA-CC are to be assembled. After such assembly, Figs.  
9 8.060101AA-CC provide a circuit drawing of a TX phase/frequency  
10 detector "txpfdet" included in the circuit of Figs. 8.0601AA-BB.

11 Fig. 8.060102 is a graph illustrating how Figs.  
12 8.060102AA-BB are to be assembled. After such assembly, Figs.  
13 8.060102AA-BB provide a circuit drawing of a TX PLL charge pump  
14 "txchgump" included in the circuit of Figs. 8.0601AA-BB.

15 Fig. 8.060103 is a graph illustrating how Figs.  
16 8.060103AA-CB are to be assembled. After such assembly, Figs.  
17 8.060103AA-CB provide a circuit drawing of a TX PLL loop filter  
18 "txloopfilter" included in the circuit of Figs. 8.0601AA-BB.

19 Fig. 8.060104 is a graph illustrating how Figs.  
20 8.060104AA-DC are to be assembled. After such assembly, Figs.  
21 8.060104AA-DC provide a circuit drawing of a TX VCO "txvco" included  
22 in the circuit of Figs. 8.0601AA-BB.

23 Fig. 8.06010401 is a graph illustrating how  
24 Figs. 8.06010401AA-BD are to be assembled. After such assembly, Figs.

FIG. 8.0601040101

8.06010401AA-BD provide a circuit drawing of a TX VCO stage "txvcostage" included in the circuit of Figs. 8.060104AA-DC.

Fig. 8.0601040101 is a graph illustrating how Figs. 8.0601040101AA-BC are to be assembled. After such assembly, Figs. 8.0601040101AA-BC provide a layout plot showing how the components of the VCO stage are laid out.

Fig. 8.060105 is a graph illustrating how Figs. 8.060105AA-DD are to be assembled. After such assembly, Figs. 8.060105AA-DD provide a circuit drawing of a divider "txdivider" included in the circuit of Figs. 8.0601AA-BB.

Fig. 8.06010501 is a graph illustrating how Figs. 8.06010501AA-AB are to be assembled. After such assembly, Figs. 8.06010501AA-AB provide a circuit drawing of a divider flip-flop "txdivtff" included in the circuit of Figs. 8.060105AA-DD.

Fig. 8.0602 is a graph illustrating how Figs. 8.0602AA-AB are to be assembled. After such assembly, Figs. 8.0602AA-AB provide a circuit drawing of a test mode data selector "txdatasel" included in the circuit of Figs. 8.06AA-ED.

Fig. 8.0603 is a graph illustrating how Figs. 8.0603AA-AB are to be assembled. After such assembly, Figs. 8.0603AA-AB provide a circuit drawing of a BPSK modulation driver "txbpsk" included in the circuit of Figs. 8.06AA-ED.

Fig. 8.0604 is a graph illustrating how Figs. 8.0604AA-AB are to be assembled. After such assembly, Figs.

8.0604AA-AB provide a circuit drawing of a frequency doubler "txdoubler" included in the circuit of Figs. 8.06AA-ED.

Fig. 8.060401 is a graph illustrating how Figs. 8.060401AA-FE are to be assembled. After such assembly, Figs. 8.060401AA-FE provide a circuit drawing of a frequency doubler core "txfdbl" included in the circuit of Figs. 8.0604AA-ED.

Fig. 8.0605 is a graph illustrating how Figs. 8.0605AA-AB are to be assembled. After such assembly, Figs. 8.0605AA-AB provide a circuit drawing of a second frequency doubler "txdoubler2" included in the circuit of Figs. 8.06AA-ED.

Fig. 8.060501 is a graph illustrating how Figs. 8.060501AA-CD are to be assembled. After such assembly, Figs. 8.060501AA-CD provide a circuit drawing of doubler driver amps "txfdbldrv" included in the circuit of Figs. 8.0605AA-CD.

Fig. 8.060502 is a graph illustrating how Figs. 8.060502AA-CD are to be assembled. After such assembly, Figs. 8.060502AA-CD provide a circuit drawing of second doubler driver amps "txfdbldrv2" included in the circuit of Figs. 8.0605AA-CD.

Fig. 8.060503 is a graph illustrating how Figs. 8.060503AA-FE are to be assembled. After such assembly, Figs. 8.060503AA-FE provide a circuit drawing of a frequency doubler core "txfdbl2" included in the circuit of Figs. 8.0605AA-CD.

Fig. 8.0606 is a graph illustrating how Figs. 8.0606AA-IE are to be assembled. After such assembly, Figs.

1 8.0606AA-IE provide a circuit drawing of a transmitter power amp  
2 "txpoweramp" included in the circuit of Figs. 8.06AA-ED.

3 Fig. 8.0607 is a graph illustrating how Figs.  
4 8.0607AA-JJ are to be assembled. After such assembly, Figs.  
5 8.0607AA-JJ provide a circuit drawing of a transmitter bias generator  
6 "txbias" included in the circuit of Figs. 8.06AA-ED.

7 Fig. 8.0608 is a graph illustrating how Figs.  
8 8.0608AA-BB are to be assembled. After such assembly, Figs.  
9 8.0608AA-BB provide a circuit drawing of a modulated backscatter  
10 transmitter "txmbs" included in the circuit of Figs. 8.06AA-ED.

11 Fig. 8.07 is a graph illustrating how Figs. 8.07AA-BB are to  
12 be assembled. After such assembly, Figs. 8.07AA-BB provide a partial  
13 circuit drawing of a 915 MHZ transmitter "tx915" included in the circuit  
14 of Figs. 8AA-CB in place of the transmitter "tx" in an alternative  
15 embodiment of the invention.

16 Fig. 8.0701 is a graph illustrating how Figs.  
17 8.0701AA-CB are to be assembled. After such assembly, Figs.  
18 8.0701AA-CB provide a circuit drawing of a TX VCO stage  
19 "txvcostage915" for use with the 915 MHZ transmitter "tx915" of  
20 Fig. 8.07 in place of the TX VCO "txvco" of Fig. 8.060104.

21 Fig. 9 is a graph illustrating how Figs. 9AA-CB are to be  
22 assembled. After such assembly, Figs. 9AA-CB provide a circuit drawing  
23 of an analog processor "anlgproc" included in the circuit of  
24 Figs. 6AA-EK.



Fig. 9.01 is a graph illustrating how Figs. 9.01AA-DH are to be assembled. After such assembly, Figs. 9.01AA-DH provide a circuit drawing of an algorithmic A/D converter with databus interface "ada\_new" included in the circuit of Figs. 9AA-CB.

Fig. 9.0101 is a graph illustrating how Figs. 9.0101AA-CK are to be assembled. After such assembly, Figs. 9.0101AA-CK provide a circuit drawing of a differential I/O op-amp "dopamp" included in the circuit of Figs. 9.01AA-DH.

Fig. 9.0102 provides a circuit drawing of an analog divider (divide by two) "adaprescale" included in the circuit of Figs. 9.01AA-DH.

Fig. 9.0103 is a graph illustrating how Figs. 9.0103AJ-FP are to be assembled. After such assembly, Figs. 9.0103AJ-FP provide a circuit drawing of a control PLA "adactl\_new" included in the circuit of Figs. 9.01AA-DH.

Fig. 9.010301 is a graph illustrating how Figs. 9.010301AA-CC are to be assembled. After such assembly, Figs. 9.010301AA-CC provide a circuit drawing of a clock generator "adacgen\_new" included in the circuit of Figs. 9.0103AJ-FP.

Fig. 9.010302 is a graph illustrating how Figs. 9.010302AA-AB are to be assembled. After such assembly, Figs. 9.010302AA-AB provide a circuit drawing of a control output driver "adacdrv\_new" included in the circuit of Figs. 9.0103AJ-FP.

1 Fig. 9.010303 is a graph illustrating how Figs.  
2 9.010303AA-AB are to be assembled. After such assembly, Figs.  
3 9.010303AA-AB provide a circuit drawing of a control output driver  
4 "adacdrvn\_new" included in the circuit of Figs. 9.0103AJ-FP.

5 Fig. 9.010304 is a graph illustrating how Figs.  
6 9.010304AA-BB are to be assembled. After such assembly, Figs.  
7 9.010304AA-BB provide a circuit drawing of a data latch "adadlat\_new"  
8 included in the circuit of Figs. 9.0103AJ-FP.

9 Fig. 9.0104 is a graph illustrating how Figs.  
10 9.0104AA-DD are to be assembled. After such assembly, Figs.  
11 9.0104AA-DD provide a circuit drawing of an analog bias circuit  
12 "adabias\_new" included in the circuit of Figs. 9.01AA-DH.

13 Fig. 9.02 is a graph illustrating how Figs. 9.02AA-DK are  
14 to be assembled. After such assembly, Figs. 9.02AA-DK provide a  
15 circuit drawing of a Vdd power up detector "pup" included in the  
16 circuit of Figs. 9AA-CB.

17 Fig. 9.03 is a graph illustrating how Figs. 9.03AA-BB are to  
18 be assembled. After such assembly, Figs. 9.03AA-BB provide a circuit  
19 drawing of a master bias source "mbs" included in the circuit of  
20 Figs. 9AA-CB.

21 Fig. 9.0301 is a graph illustrating how Figs.  
22 9.0301AA-DJ are to be assembled. After such assembly, Figs.  
23 9.0301AA-DJ provide a circuit drawing of a band gap reference  
24 generator "mbs\_bgr" included in the circuit of Figs. 9.03AA-BB.

FIG. 9.0302

Fig. 9.0302 is a graph illustrating how Figs. 9.0302AA-DI are to be assembled. After such assembly, Figs. 9.0302AA-DI provide a circuit drawing of a temperature compensated current generator "mbs\_cur" included in the circuit of Figs. 9.03AA-BB.

Fig. 9.0303 is a graph illustrating how Figs. 9.0303AA-CF are to be assembled. After such assembly, Figs. 9.0303AA-CF provide a circuit drawing of a reference current generator "mbs\_iref" included in the circuit of Figs. 9.03AA-BB.

Fig. 9.04 is a graph illustrating how Figs. 9.04AA-CE are to be assembled. After such assembly, Figs. 9.04AA-CE provide a circuit drawing of a voltage regulator "vrg" included in the circuit of Figs. 9AA-CB.

Fig. 9.05 is a graph illustrating how Figs. 9.05AA-FE are to be assembled. After such assembly, Figs. 9.05AA-FE provide a circuit drawing of a voltage regulator "vrgtx" included in the circuit of Figs. 9AA-CB.

Fig. 9.0501 is a graph illustrating how Figs. 9.0501AA-CD are to be assembled. After such assembly, Figs. 9.0501AA-CD provide a circuit drawing of an operational amplifier without compensation "opampnc" included in the circuit of Figs. 9.05AA-FE.

Fig. 9.06 is a graph illustrating how Figs. 9.06AA-DD are to be assembled. After such assembly, Figs. 9.06AA-DD provide a

1 circuit drawing of a bias OK detector "biasok" included in the circuit  
2 of Figs. 9AA-CB.

3 Fig. 9.07 is a graph illustrating how Figs. 9.07AA-EG are  
4 to be assembled. After such assembly, Figs. 9.07AA-EG provide a  
5 circuit drawing of an analog port current source "aportcs" included in  
6 the circuit of Figs. 9AA-CB.

7 Fig. 9.08 is a graph illustrating how Figs. 9.08AA-CC are  
8 to be assembled. After such assembly, Figs. 9.08AA-CC provide a  
9 circuit drawing of an analog multiplexer decoder "asl" included in the  
10 circuit of Figs. 9AA-CB.

11 Fig. 9.09 is a graph illustrating how Figs. 9.09AA-BB are to  
12 be assembled. After such assembly, Figs. 9.09AA-BB provide a circuit  
13 drawing of a random clock generator "rcg" included in the circuit of  
14 Figs. 9AA-CB.

15 Fig. 9.0901 is a graph illustrating how Figs.  
16 9.0901AA-CH are to be assembled. After such assembly, Figs.  
17 9.0901AA-CH provide a circuit drawing of a linear feedback shift  
18 register "rcg\_sreg" included in the circuit of Figs. 9.09AA-CB.

19 Fig. 9.090101 is a graph illustrating how Figs.  
20 9.090101AA-CC are to be assembled. After such assembly, Figs.  
21 9.090101AA-CC provide a circuit drawing of a shift register bit  
22 "rcg\_sregbit0" included in the circuit of Figs. 9.0901AA-CH.

23 Fig. 9.090102 is a graph illustrating how Figs.  
24 9.090102AA-BB are to be assembled. After such assembly, Figs.

1 9.090102AA-BB provide a circuit drawing of a shift register bit  
2 "rcg\_sregbit" included in the circuit of Figs. 9.0901AA-CH.

3 Fig. 9.0902 is a graph illustrating how Figs.  
4 9.0902AA-FL are to be assembled. After such assembly, Figs.  
5 9.0902AA-FL provide a circuit drawing of a low power oscillator and  
6 bias generator "rcg\_osc" included in the circuit of Figs. 9.09AA-CB.

7 Fig. 9.0903 is a graph illustrating how Figs.  
8 9.0903AA-CC are to be assembled. After such assembly, Figs.  
9 9.0903AA-CC provide a circuit drawing of a clock generator "rcg\_clkgen"  
10 included in the circuit of Figs. 9.09AA-CB.

11 Fig. 10 is a graph illustrating how Figs. 10AA-DD are to be  
12 assembled. After such assembly, Figs. 10AA-DD provide a circuit  
13 drawing of a pn processor "pnproc" included in the circuit of  
14 Figs. 6AA-EK.

15 Fig. 10.01 is a graph illustrating how Figs. 10.01AA-DI are  
16 to be assembled. After such assembly, Figs. 10.01AA-DI provide a  
17 circuit drawing of a digital PN correlator "dcorr" included in the circuit  
18 of Figs. 10AA-DI.

19 Fig. 10.0101 is a graph illustrating how Figs.  
20 10.0101AA-BG are to be assembled. After such assembly, Figs.  
21 10.0101AA-BG provide a circuit drawing of a PN correlator shift register  
22 "dcorr\_sreg" included in the circuit of Figs. 10.01AA-DI.

23 Fig. 10.010101 is a circuit drawing of a PN  
24 correlator bit "dcorr\_bit" included in the circuit of Figs. 10.0101AA-BG.

Fig. 10.01010101 is a circuit drawing of a shift register cell "dcorr\_sregbit" included in the circuit of Figs. 10.010101.

Fig. 10.0102 is a graph illustrating how Figs. 10.0102AA-CN are to be assembled. After such assembly, Figs. 10.0102AA-CN provide a circuit drawing of a correlator bias generator "dcorr\_bias" included in the circuit of Figs. 10.01AA-DI.

Fig. 10.02 is a graph illustrating how Figs. 10.02AA-BE are to be assembled. After such assembly, Figs. 10.02AA-BE provide a circuit drawing of a PN lock detector "pnlockdet" included in the circuit of Figs. 10AA-DD.

Fig. 10.0201 is a graph illustrating how Figs. 10.0201AA-AB are to be assembled. After such assembly, Figs. 10.0201AA-AB provide a circuit drawing of a counter bit "lockcounterbit" included in the circuit of Figs. 10.02AA-BE.

Fig. 10.03 is a graph illustrating how Figs. 10.03AA-AB are to be assembled. After such assembly, Figs. 10.03AA-AB provide a circuit drawing of a PN generator clock "pngclk" included in the circuit of Figs. 10AA-DD.

Fig. 10.04 is a graph illustrating how Figs. 10.04AA-CE are to be assembled. After such assembly, Figs. 10.04AA-CE provide a circuit drawing of a PN generator shift register "pngshr" included in the circuit of Figs. 10 AA-DD.

1 Fig. 10.0401 is a circuit drawing of a PN generator  
2 shift register cell "pngsreg" included in the circuit of Figs. 10.04AA-CE.

3 Fig. 10.0402 is a graph illustrating how Figs.  
4 10.0402AA-CB are to be assembled. After such assembly, Figs.  
5 10.0402AA-CB provide a circuit drawing of a PN generator shift register  
6 summer "pngssum" included in the circuit of Figs. 10.04AA-CE.

7 Fig. 10.05 is a circuit drawing of a PN controller D type  
8 flip-flop "pnddff" included in the circuit of Figs. 10AA-DD.

9 Fig. 10.06 is a graph illustrating how Figs. 10.06AA-DH are  
10 to be assembled. After such assembly, Figs. 10.06AA-DH provide a  
11 circuit drawing of differential and PN encoder "dpenc" included in the  
12 circuit of Figs. 10AA-DD.

13 Fig. 10.07 is a graph illustrating how Figs. 10.07AA-CD are  
14 to be assembled. After such assembly, Figs. 10.07AA-CD provide a  
15 circuit drawing of a PSK/FSK generator "fskgen" included in the circuit  
16 of Figs. 10AA-DD.

17 Fig. 10.0701 is a graph illustrating how Figs.  
18 10.0701AA-AB are to be assembled. After such assembly, Figs.  
19 10.0701AA-AB provide a circuit drawing of a FSK counter bit "fskcbt"  
20 included in the circuit of Figs. 10AA-DD.

21 Fig. 11 is a graph illustrating how Figs. 11AA-AB are to be  
22 assembled. After such assembly, Figs. 11AA-AB provide a circuit  
23 drawing of a battery I/O buffer "batalg" included in the circuit of  
24 Figs. 6AA-EK.

Fig. 12 is a graph illustrating how Figs. 12AA-AB are to be assembled. After such assembly, Figs. 12AA-AB provide a circuit drawing of a digital I/O pad buffer "paddig" included in the circuit of Figs. 6AA-EK.

Fig. 13 is a circuit drawing of a digital input pad buffer "paddigin" included in the circuit of Figs. 6AA-EK.

Fig. 13.5 is a circuit drawing of a digital input pad buffer "paddigin2" included in the circuit of Figs. 6AA-EK.

Fig. 14 is a circuit drawing of an analog I/O pad buffer "padalg" included in the circuit of Figs. 6AA-EK.

Fig. 15 is a graph illustrating how Figs. 15AA-BC are to be assembled. After such assembly, Figs. 15AA-BC provide a circuit drawing of return link configuration control logic "rlconfig" included in the circuit of Figs. 6AA-EK.

Fig. 16 is a graph illustrating how Figs. 16AA-EH are to be assembled. After such assembly, Figs. 16AA-EH provide a circuit drawing of a temperature sensor "tsn" included in the circuit of Figs. 6AA-EK.

Fig. 16.01 is a graph illustrating how Figs. 16.01AA-DI are to be assembled. After such assembly, Figs. 16.01AA-DI provide a circuit drawing of an operational amplifier "opamp" included in the circuit of Figs. 16AA-EH.

Fig. 17 is a graph illustrating how Figs. 17AA-BB are to be assembled. After such assembly, Figs. 17AA-BB provide a circuit



1 drawing of a magnetic field sensor "mag" (a sensor for sensing magnetic  
2 fields) included in the circuit of Figs. 6AA-EK.

3 Fig. 18 is a graph illustrating how Figs. 18AA-AB are to be  
4 assembled. After such assembly, Figs. 18AA-AB provide a circuit  
5 drawing of a chip bypass capacitor "bypcap3" included in the circuit of  
6 Figs. 6AA-EK.

7 Fig. 19 is a graph illustrating how Figs. 19AA-EK are to be  
8 assembled. After such assembly, Figs. 19AA-EK provide a circuit  
9 drawing of a monolithic semiconductor integrated circuit "LO3BT3F" in  
10 accordance with an alternative embodiment of the invention. The  
11 integrated circuit of Figs. 19AA-EK is similar to the integrated circuit  
12 shown in Figs. 6AA-EK, like component names indicating like  
13 components, except that the integrated circuit of Figs. 19AA-EK has no  
14 ROM, and is adapted to be connected to external ROM "extrom". The  
15 embodiment of Figs. 19AA-EK is particularly useful for test purposes.

16 Fig. 20 is a graph illustrating how Figs. 20AA-DF are to be  
17 assembled. After such assembly, Figs. 20AA-DF provide a circuit  
18 drawing of a data processor "dataproc\_t3" to be used in the integrated  
19 circuit of Fig. 19 in place of the data processor "dataproc" of Fig. 7.

20 Fig. 20.01 is a graph illustrating how Figs. 20.01AA-CB are  
21 to be assembled. After such assembly, Figs. 20.01AA-CB provide a  
22 circuit drawing of an external ROM "extrom" shown in Figs. 20AA-CB.

23 Fig. 20.0101 is a graph illustrating how Figs.  
24 20.0101AA-BB are to be assembled. After such assembly, Figs.

1 20.0101AA-BB provide a circuit drawing of external ROM control logic  
2 "extromctl" included in the circuit of Figs. 20.01AA-CB.

3 Fig. 20.0102 is a circuit drawing of an external ROM  
4 address interface "extromad" included in the circuit of Figs. 20.01AA-CB.

5 Fig. 20.0103 is a graph illustrating how Figs.  
6 20.0103AA-AC are to be assembled. After such assembly, Figs.  
7 20.0103AA-AC provide a circuit drawing of a digital I/O pad buffer  
8 "paddigt3" included in the circuit of Figs. 20.01AA-CB.

9 Fig. 20.0104 is a circuit drawing of an external ROM  
10 databus interface "extromdb" included in the circuit of Figs. 20.01AA-CB.

11 Fig. 21 is a circuit schematic illustrating a transmitter switchable  
12 between an active mode and a backscatter mode, and employing  
13 separate antennas for the active mode and the backscatter mode.

14 Fig. 22 is a circuit schematic illustrating a transmitter switchable  
15 between an active mode and a backscatter mode, and employing the  
16 same antenna for both the active mode and the backscatter mode.

17 Fig. 23 is a circuit schematic illustrating low battery detection  
18 circuitry.

19 Fig. 24 is a circuit schematic illustrating circuitry providing a low  
20 power wake up timer.

21 Figs. 25-26 provide a flowchart illustrating logic employed for  
22 switching between a low power sleep mode, and higher power modes.

23 Fig. 27 is a diagram of current versus time illustrating switching  
24 between a low power sleep mode, and higher power modes.



1 Fig. 37 is a circuit schematic of an inverter illustrating a power  
2 saving technique employed in a pseudo random number generator  
3 embodying one aspect of the invention.

4 Fig. 38 is a cross-sectional view illustrating a step of a process  
5 of manufacturing a Schottky diode.

6 Fig. 39 is a cross-sectional view illustrating a step subsequent to  
7 the step of Fig. 38.

8 Fig. 40 is a cross-sectional view illustrating a step subsequent to  
9 the step of Fig. 39.

10 Fig. 41 is a cross-sectional view illustrating a step subsequent to  
11 the step of Fig. 40.

12 Fig. 42 is a top view illustrating a step subsequent to the step  
13 of Fig. 41 and showing parallel connection of some Schottky diodes of  
14 a plurality of Schottky diodes.

15 Fig. 43 is a top view illustrating a step subsequent to the step  
16 of Fig. 41 in accordance with an alternative embodiment of the  
17 invention and showing parallel connection of all Schottky diodes of a  
18 plurality of Schottky diodes.

19 Fig. 44 is a cross-sectional view illustrating a step of an  
20 alternative process of manufacturing a Schottky diode.

21 Fig. 45 is a cross-sectional view illustrating a step subsequent to  
22 the step of Fig. 44.

23 Fig. 46 is a cross-sectional view illustrating a step subsequent to  
24 the step of Fig. 45.

1 Fig. 47 is a cross-sectional view illustrating a step subsequent to  
2 the step of Fig. 46.

3 Fig. 48 is a simplified circuit schematic of a quick bias AC-  
4 coupled video amplifier included in the integrated circuit.

5 Fig. 49 is a plot of voltage versus angular frequency illustrating  
6 selection of components to realize a desired high pass roll off frequency  
7 in the amplifier of Fig. 48.

8 Fig. 50 is a simplified circuit schematic illustrating sharing of a  
9 single antenna by both a Schottky detector and an active transmitter.

10 Fig. 51 is a simplified circuit schematic illustrating circuitry  
11 included in the active transmitter of Fig. 50 in accordance with one  
12 aspect of the invention.

13 Fig. 52 is a simplified circuit schematic illustrating sharing of a  
14 single antenna by both a Schottky detector and a backscatter  
15 transmitter.

16 Fig. 53 is a simplified circuit schematic illustrating sharing of a  
17 single antenna by both a Schottky detector and a backscatter transmitter  
18 in accordance with an alternative embodiment of the invention.

19 Fig. 54 is a graph of voltage versus time illustrating a method of  
20 determining when frequency lock has occurred.

21 Fig. 55 is a flowchart illustrating a top level of code stored in  
22 ROM in the integrated circuit.

23 Figs. 56A and B define a flowchart illustrating a command  
24 processing routine performed by the integrated circuit.

1 Figs. 57A and B define a flowchart illustrating steps performed  
2 by the integrated circuit in response to an Identify command received  
3 from the interrogator in which the interrogator requests, via radio  
4 frequency command, identification of an integrated circuit.

5 Fig. 58 is a flowchart illustrating steps performed to initialize the  
6 interrogator.

7 Fig. 59 is a flowchart illustrating steps performed when the  
8 interrogator sends a command to the integrated circuit.

9 Fig. 60 is a flowchart illustrating steps performed by the  
10 interrogator in issuing an Identify command.

11 Fig. 61 is a simplified circuit diagram of a digital clock recovery  
12 loop including a start-up circuit including a counter, a voltage controlled  
13 oscillator, a charge pump and loop filter, and a state machine. The  
14 start-up circuit and counter determine when clock frequency is close to  
15 a desired value.

16 Fig. 62 is a plot of frequency produced by a voltage controlled  
17 oscillator versus control voltage applied to the voltage controlled  
18 oscillator.

19 Fig. 63 is a timing diagram showing when the start-up circuit of  
20 Fig. 61 issues pump up signals to increase the control voltage applied  
21 to the voltage controlled oscillator.

22 Fig 64 is a state diagram illustrating the design of the state  
23 machine of Fig. 61.

1 Figs. 65-70 illustrate steps used in designing a state machine that  
2 implements the state diagram of Fig. 64. Fig. 65 illustrates flip-flops  
3 having outputs representing in binary form the various states of the  
4 state diagrams and having inputs representing next state values. Fig.  
5 66 is a state table. Figs. 67 and 68 are Karnaugh maps used to  
6 derive minimum logic circuitry needed to derive circuit output functions  
7 and flip-flop input functions.

8 Fig. 71 is a simplified timing diagram illustrating operation of the  
9 state machine.

10 Fig. 72 is a table illustrating step sizes produced by the start-up  
11 circuit and the state machine.

## 12 SUMMARY OF THE INVENTION

13 The invention provides a radio frequency identification device  
14 comprising an integrated circuit including a receiver, a transmitter, and  
15 a microprocessor. The integrated circuit is preferably a monolithic  
16 single die integrated circuit including the receiver, the transmitter, and  
17 the microprocessor. Because the device includes an active transponder,  
18 instead of a transponder which relies on magnetic coupling for power,  
19 the device has a much greater range.  
20

21 One aspect of the invention provides a radio frequency  
22 identification device comprising a monolithic integrated circuit including  
23 a receiver, a transmitter which can operate at frequencies above 400  
24 MHz, and a microprocessor.

1 Another aspect of the invention provides a radio frequency  
2 identification device comprising a monolithic integrated circuit including  
3 a receiver, a transmitter which can operate at frequencies above 1 GHz,  
4 and a microprocessor.

5 Another aspect of the invention provides a radio frequency  
6 identification device comprising a monolithic integrated circuit including  
7 a transmitter, a microprocessor, and a receiver which can receive and  
8 interpret signals having frequencies above 400 MHz.

9 Another aspect of the invention provides a radio frequency  
10 identification device comprising a monolithic integrated circuit including  
11 a transmitter, a microprocessor, and a receiver which can receive and  
12 interpret signals having frequencies above 1 Ghz.

13 Another aspect of the invention provides a radio frequency  
14 identification device comprising a monolithic integrated circuit including  
15 a receiver, a microwave transmitter, and a microprocessor.

16 Another aspect of the invention provides a radio frequency  
17 identification device comprising a monolithic integrated circuit including  
18 a microwave receiver, a transmitter, and a microprocessor.

19 Another aspect of the invention provides a radio frequency  
20 identification device comprising a single die including a receiver, a  
21 transmitter, and a microprocessor, the die having a size less than 90,000  
22 mils<sup>2</sup>. In accordance with a more preferred embodiment of the  
23 invention, the die has a size less than 300 x 300 mils<sup>2</sup>. In accordance  
24 with a more preferred embodiment of the invention, the die has a size



1 less than 37,500 mils<sup>2</sup>. In accordance with a more preferred  
2 embodiment of the invention, the die has a size of 209 by 116 mils<sup>2</sup>.

3 Another aspect of the invention provides a radio frequency  
4 identification device comprising a single die integrated circuit including  
5 a receiver, a transmitter, and a microprocessor.

6 Another aspect of the invention provides a radio frequency  
7 identification device comprising a single die with a single metal layer  
8 including a receiver, a transmitter, and a microprocessor.

9 Another aspect of the invention provides a radio frequency  
10 identification device comprising a single die integrated circuit including  
11 a receiver, a transmitter, and a microprocessor formed using a single  
12 metal layer processing method.

13 Another aspect of the invention provides a radio frequency  
14 identification system comprising an integrated circuit including a receiver,  
15 and a transmitter; and an antenna coupled to the integrated circuit, the  
16 integrated circuit being responsive to radio frequency signals of multiple  
17 carrier frequencies.

18 Another aspect of the invention provides a radio frequency  
19 identification device comprising transponder circuitry formed in a  
20 monolithic integrated circuit comprising both transmitting and receiving  
21 circuits of the transponder circuitry; a power supply operably associated  
22 with the transponder circuitry; and an antenna operably associated with  
23 the transponder circuitry.  
24

1 Another aspect of the invention provides a radio frequency  
2 identification device comprising a monolithic semiconductor integrated  
3 circuit including a receiver and a transmitter; means for applying a  
4 supply of power to the integrated circuit device from a battery; and  
5 means for configuring the integrated circuit to receive and transmit  
6 radio frequency signals.

7 Another aspect of the invention provides a method for producing  
8 a radio frequency identification device, the method comprising the  
9 following steps: providing a monolithic integrated circuit having a  
10 receiver and a transmitter; and providing a package configured to carry  
11 the integrated circuit.

12 Another aspect of the invention provides a method for adapting  
13 a radio frequency data communication device for use at a desired  
14 carrier frequency for use in a radio frequency identification (RFID)  
15 device, the method comprising the following steps: providing an  
16 integrated circuit having tunable circuitry, the integrated circuit  
17 comprising a receiver and a transmitter; configuring the integrated circuit  
18 for connection with a power supply to enable operation; configuring the  
19 integrated circuit to receive and apply radio frequency signals via an  
20 antenna, the antenna and the tunable circuitry cooperating in operation  
21 there between; and tuning the tunable circuitry and the antenna to  
22 realize a desired carrier frequency from a wide range of possible carrier  
23 frequencies. A method for adapting a radio frequency data  
24 communication device for use at a desired carrier frequency for use in

1 a radio frequency identification device, the method comprising the  
2 following steps: providing an integrated circuit having tunable circuitry,  
3 the integrated circuit comprising a receiver and a transmitter; configuring  
4 the integrated circuit for connection with a power supply to enable  
5 operation; configuring the integrated circuit to receive and apply radio  
6 frequency signals via an antenna, the antenna and the tunable circuitry  
7 cooperating in operation there between; and tuning the antenna to  
8 realize a desired carrier frequency from a wide range of possible carrier  
9 frequencies.

10 Another aspect of the invention provides a radio frequency  
11 communications device comprising an integrated circuit including a  
12 transmitter and a receiver, the integrated circuit including a clock  
13 recovery circuit recovering a clock frequency from a signal received by  
14 the receiver, the clock recovery circuit having a phase lock loop  
15 including a voltage controlled oscillator, and a loop filter having a  
16 capacitor storing a voltage indicative of a frequency at which the  
17 voltage controlled oscillator is oscillating, the integrated circuit using the  
18 voltage stored on the capacitor to generate a clock frequency for the  
19 transmitter.

20 Another aspect of the invention provides a method of recovering  
21 a clock frequency from a received radio frequency signal, storing the  
22 clock frequency, and using the clock frequency for radio frequency  
23 transmission by a transmitter, the method comprising: providing a clock  
24 recovery circuit recovering a clock frequency from a signal received by

1 the receiver, the clock recovery circuit having a phase lock loop  
2 including a voltage controlled oscillator, and a loop filter having a  
3 capacitor; using the clock recovery circuit to recover a clock frequency  
4 from a received radio frequency signal; storing on the capacitor a  
5 voltage indicative of frequency at which the voltage controlled oscillator  
6 is oscillating; using the voltage stored on the capacitor to generate a  
7 clock frequency for use by the transmitter.

8 Another aspect of the invention provides a method of recovering  
9 and storing a clock frequency from a received radio frequency signal in  
10 a radio frequency identification device including a transmitter and a  
11 receiver, the method comprising providing a clock recovery circuit  
12 recovering a clock frequency from a signal received by the receiver, the  
13 clock recovery circuit having a phase lock loop; using the clock recovery  
14 circuit to recover a clock frequency from a received radio frequency  
15 signal; storing in analog form a value indicative of frequency at which  
16 the voltage controlled oscillator is oscillating; and using the analog value  
17 to generate a clock frequency for use by the transmitter.

18 Another aspect of the invention provides a radio frequency  
19 communications device comprising an integrated circuit including a  
20 transmitter and a receiver, the transmitter being switchable between a  
21 backscatter mode, wherein a carrier for the transmitter is derived from  
22 a carrier received from an interrogator spaced apart from the radio  
23 frequency communications device, and an active mode, wherein a carrier  
24 for the transmitter is generated by the integrated circuit itself.

1 Another aspect of the invention provides a radio frequency  
2 communications device comprising an integrated circuit including a  
3 transmitter and a receiver, the transmitter selectively transmitting a  
4 signal using a modulation scheme, the transmitter being switchable for  
5 transmission using different modulation schemes.

6 Another aspect of the invention provides a method for adapting  
7 modulation schemes of a radio frequency data communication device in  
8 a radio frequency identification device, the method comprising the  
9 following steps: providing an integrated circuit having switching circuitry,  
10 a receiver, a transmitter, and a processor; the integrated circuit having  
11 a plurality of transmitting circuits including a first transmitting circuit  
12 configured to realize an active transmitter scheme and a second  
13 transmitting circuit configured to realize a modulated backscatter scheme;  
14 configuring the integrated circuit for connection with a power supply to  
15 enable operation; configuring the integrated circuit to receive and apply  
16 radio frequency signals via an antenna, the antenna and the tunable  
17 circuitry cooperating in operation; and switching the switchable circuitry  
18 with respect to the antenna to enable one of the transmitting circuits  
19 to realize one of the modulation schemes.

20 Another aspect of the invention provides a method for adapting  
21 modulation schemes of a radio frequency data communication device in  
22 a radio frequency identification device, the method comprising the  
23 following steps: providing an integrated circuit having switching circuitry,  
24 a receiver, a transmitter, and a processor, the integrated circuit

1 including a plurality of transmitting circuits, the plurality of transmitting  
2 circuits configured to selectively realize a plurality of modulated  
3 backscatter schemes; configuring the integrated circuit for connection  
4 with a power supply to enable operation; configuring the integrated  
5 circuit to receive and apply radio frequency signals via an antenna, the  
6 antenna and the tunable circuitry cooperating in operation; and switching  
7 the transmitting circuits with respect to the antenna to enable one of  
8 the transmitting circuits to realize one of the modulation schemes.

9 Another aspect of the invention provides a radio frequency  
10 identification device comprising: an integrated circuit including a  
11 transmitter and a receiver, the integrated circuit being adapted to be  
12 connected to a battery, and further including a comparator comparing  
13 the voltage of the battery with a predetermined voltage and generating  
14 a low battery signal if the voltage of the battery is less than the  
15 predetermined voltage.

16 Another aspect of the invention provides a method for detecting  
17 a low battery condition in a radio frequency data communication device  
18 for use in a radio frequency identification device, the method comprising  
19 the following steps: providing an integrated circuit having switching  
20 circuitry, a receiver, and a transmitter, the integrated circuit including  
21 a comparator configured to compare the battery voltage with a  
22 predetermined voltage and generate a low battery signal if the battery  
23 voltage is less than the predetermined voltage; configuring the integrated  
24 circuit for connection with the battery to enable operation; configuring

the integrated circuit to receive and apply radio frequency signals via an antenna, the antenna and the tunable circuitry cooperating in operation there between; determining a predetermined voltage for the battery; comparing the voltage of the battery with the predetermined voltage; and generating a low battery signal if the voltage of the battery is less than the predetermined voltage.

Another aspect of the invention provides a radio frequency communications device comprising an integrated circuit including a transmitter and a receiver, the integrated circuit periodically checking if a radio frequency signal is being received by the receiver, the integrated circuit further including a timer setting a time period for the checking, the timer having a frequency lock loop.

Another aspect of the invention provides a radio frequency communications device comprising an integrated circuit including a transmitter and a receiver, the integrated circuit being configured to periodically check if a radio frequency signal is being received by the receiver, the integrated circuit further including a timer setting a time period for the checking, the timer having a phase lock loop.

Another aspect of the invention provides a method for calibrating a clock in a radio frequency data communication device for use in a radio frequency identification device, the method comprising the following steps: providing an integrated circuit having a receiver and a transmitter, the integrated circuit including a timer having a frequency lock loop configured to set a time period for periodically checking if

1 a radio frequency signal is being received by the receiver; configuring  
2 the integrated circuit for connection with a battery to enable operation;  
3 configuring the integrated circuit to receive and apply radio frequency  
4 signals via an antenna, the antenna and the integrated circuit  
5 cooperating in operation therebetween; and periodically checking whether  
6 a radio frequency signal is being received by the receiver.

7 Another aspect of the invention provides a radio frequency  
8 identification device for receiving and responding to radio frequency  
9 commands from an interrogator transmitting a radio frequency signal, the  
10 device comprising an integrated circuit including a receiver, a  
11 transmitter, and a connection pin, the integrated circuit being switchable  
12 between a radio frequency receive mode wherein the receiver receives  
13 commands via radio frequency, and a direct receive mode wherein  
14 commands are received via the connection pin.

15 Another aspect of the invention provides a radio frequency  
16 identification device for receiving and responding to radio frequency  
17 commands from an interrogator transmitting a radio frequency signal, the  
18 device comprising an integrated circuit including a receiver, a  
19 transmitter, and a digital input pin, the integrated circuit being  
20 switchable between a radio frequency receive mode wherein the receiver  
21 receives commands via radio frequency, and a direct receive mode  
22 wherein commands are received digitally via the digital input pin.  
23 Another aspect of the invention provides a radio frequency identification  
24 device for receiving and responding to radio frequency commands from



an interrogator transmitting a radio frequency signal, the device comprising an integrated circuit including a receiver, a transmitter, and a connection pin, the integrated circuit being switchable between a radio frequency receive mode wherein the receiver receives commands via radio frequency, and a direct receive mode wherein a modulation signal without a carrier is received via the connection pin.

Another aspect of the invention provides a radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising an integrated circuit including a receiver, a transmitter, and a connection pin, the integrated circuit being switchable between a radio frequency transmit mode wherein the receiver transmits responses to the commands via radio frequency, and a direct transmit mode wherein responses are transmitted via the connection pin.

Another aspect of the invention provides a radio frequency identification device for receiving and responding to radio frequency commands from an interrogator transmitting a radio frequency signal, the device comprising an integrated circuit including a receiver, a transmitter, and a digital output pin, the integrated circuit being switchable between a radio frequency transmit mode wherein the receiver transmits responses to the commands via radio frequency, and a direct transmit mode wherein responses are transmitted digitally via the digital output pin.

1 Another aspect of the invention provides a radio frequency  
2 identification device for receiving and responding to radio frequency  
3 commands from an interrogator transmitting a radio frequency signal, the  
4 device comprising an integrated circuit including a receiver, a  
5 transmitter, and a connection pin, the integrated circuit being switchable  
6 between a radio frequency transmit mode wherein the receiver transmits  
7 responses to the commands via radio frequency, and a direct transmit  
8 mode wherein a modulation signal without a carrier is transmitted via  
9 the connection pin.

10 Another aspect of the invention provides a method comprising the  
11 following steps: providing an integrated circuit having a receiver, a  
12 transmitter, and a connection pin, the integrated circuit including a  
13 switchable circuit configured to switch between a radio frequency receive  
14 mode wherein the receiver receives commands via radio frequency, and  
15 a direct receive mode wherein commands are received via the  
16 connection pin; configuring the integrated circuit for connection with a  
17 battery; configuring the integrated circuit to receive and transmit radio  
18 frequency signals via an antenna, the antenna and the integrated circuit  
19 cooperating in operation; and switching to one of the radio frequency  
20 receive mode and the direct receive mode to enable receipt of radio  
21 frequency commands or commands received via the connection pin.  
22 Another aspect of the invention provides a method comprising the  
23 following steps: providing an integrated circuit having a receiver, a  
24 transmitter, and a connection pin, the integrated circuit including a

switchable circuit configured to switch between a radio frequency transmit mode wherein the transmitter transmits information via radio frequency, and a direct transmit mode wherein data is transmitted via the connection pin; configuring the integrated circuit for connection with a battery; configuring the integrated circuit to receive and transmit radio frequency signals via an antenna, the antenna and the integrated circuit cooperating in operation; and switching to one of the radio frequency transmit mode and the direct transmit mode to enable transmission of information via radio frequency or via the connection pin.

Another aspect of the invention provides an integrated circuit comprising a radio frequency receiver; a unique, non-alterable indicia identifying the integrated circuit; and a radio frequency transmitter configured to transmit a signal representative of the indicia in response to a command received by the receiver.

Another aspect of the invention provides a radio frequency identification device comprising an integrated circuit including a receiver for receiving radio frequency commands from an interrogation device, and a transmitter for transmitting a signal identifying the device to the interrogator, the transmitter and receiver being formed on a die having a lot number, wafer number, and die number, the integrated circuit including non-alterable indicia identifying the lot number, wafer number, and die number, the transmitter being configured to transmit the non-alterable indicia in response to a manufacturer's command received by

1 the receiver, the transmitted non-alterable indicia being different from  
2 the identifying signal.

3 Another aspect of the invention provides a method of tracing  
4 manufacturing process problems by tracing the origin of a defective  
5 radio frequency identification integrated circuit, the method comprising:  
6 forming a non-alterable indicia on a die for the integrated circuit, the  
7 indicia representing the wafer lot number, wafer number, and die  
8 number on the wafer, the indicia being not readily ascertainable by a  
9 user; and causing the integrated circuit to transmit the non-alterable  
10 indicia via radio frequency in response to a manufacturer's command.

11 Another aspect of the invention provides a method of tracing  
12 stolen property including a radio frequency identification integrated  
13 circuit, the method comprising: forming a non-alterable indicia on a die  
14 for the integrated circuit, the indicia representing the wafer lot number,  
15 wafer number, and die number on the wafer, the indicia being not  
16 readily ascertainable by a user; and causing the integrated circuit to  
17 transmit the non-alterable indicia via radio frequency in response to a  
18 manufacturer's command.

19 Another aspect of the invention provides a method of tracing  
20 manufacturing process problems in the manufacture of a radio frequency  
21 integrated circuit by tracing defect origin, the method comprising the  
22 following steps: providing a detectable signature on the integrated  
23 circuit, the signature indicative of one or more of the wafer lot number,  
24 wafer number, and die number of a die for the integrated circuit; and

1 enabling the integrated circuit to transmit the signature via radio  
2 frequency responsive to an inquiry command.

3 Another aspect of the invention provides a radio frequency  
4 identification device comprising: an integrated circuit including a  
5 microprocessor, a receiver receiving radio frequency commands from an  
6 interrogation device, and a transmitter transmitting a signal identifying  
7 the device to the interrogator, the integrated circuit switching between  
8 a sleep mode, and a microprocessor on mode, in which more power is  
9 consumed than in the sleep mode, if the microprocessor determines that  
10 a signal received by the receiver is a radio frequency command from  
11 an interrogation device.

12 Another aspect of the invention provides a method for conserving  
13 power during operation of a radio frequency identification device, the  
14 method comprising the following steps: providing a receiver, a  
15 transmitter, microprocessor, and wake-up circuitry, the wake-up circuitry  
16 configured to selectively supply clock signals to the processor and thus  
17 control power consumption of the processor; configuring the receiver  
18 with an antenna to receive radio frequency signals from an interrogation  
19 device; configuring the transmitter to transmit a signal identifying the  
20 device to the interrogator; selectively enabling powered wake-up of the  
21 receiver to periodically check for presence of radio frequency signals;  
22 detecting whether a radio frequency signal is valid; and depending on  
23 whether a radio frequency signal is valid, supplying clock signals to the  
24 processor.



performing the following tests to determine whether to further switch to a microprocessor on mode because a valid radio frequency signal is present: (a) determining if any radio frequency signal is present and, if so, proceeding to step (b); and, if not, returning to the sleep mode; and (b) determining if the radio frequency signal has a predetermined number of transitions per a predetermined time period of time and, if so, switching to the microprocessor on mode; and, if not, returning to the sleep mode.

Another aspect of the invention provides a radio frequency identification device switchable between a sleep mode and a mode in which more power is consumed than in the sleep mode, the radio frequency identification device comprising a transponder including a receiver and a transmitter; means for periodically checking whether any radio frequency signal is being received by the receiver; and means for determining if a radio frequency signal has a predetermined number of transitions within a predetermined period of time.

<sup>Sub A2</sup> Another aspect of the invention provides a method for conserving power in a radio frequency identification device, the method comprising periodically switching from a sleep mode to a receiver on mode and performing the following tests to determine whether to further switch to a microprocessor on mode because a valid radio frequency signal is present: (a) determining if any radio frequency signal is present and, if so, proceeding to step (b); and, if not, returning to the sleep mode; (b) determining if the radio frequency signal is modulated and has a

1 predetermined number of transitions per a predetermined period of time  
2 and, if so, proceeding to step (c); and, if not, returning to the sleep  
3 mode; and © determining if the modulated radio frequency signal has  
4 a predetermined number of transitions per a predetermined period of  
5 time different from the predetermined time of step (b) and, if so,  
6 switching to the microprocessor on mode; and, if not, returning to the  
7 sleep mode.

8 Another aspect of the invention provides a method of forming an  
9 integrated circuit including a Schottky diode, the method comprising:  
10 providing a p-type substrate; defining an n-type region relative to the  
11 substrate; forming an insulator over the n-type region; removing an area  
12 of the insulator for definition of a contact hole, and removing an area  
13 encircling the contact hole; forming n+regions in the n-type regions  
14 encircling the contact hole; depositing a Schottky metal in the contact  
15 hole; and annealing the metal to form a silicide interface to the n-type  
16 region.

17 Another aspect of the invention provides a method of forming an  
18 integrated circuit including a Schottky diode, the method comprising:  
19 providing a substrate; defining a p-type region relative to the substrate;  
20 forming an insulator over the p-type region; removing an area of the  
21 insulator for definition of a contact hole, and removing an area  
22 encircling the contact hole; forming p+regions in the p-type regions  
23 encircling the contact hole; depositing a Schottky metal in the contact  
24





1 Another aspect of the invention provides an integrated circuit for  
2 radio frequency communications comprising an inductorless radio  
3 frequency detector.

4 Another aspect of the invention provides a system comprising an  
5 antenna; a transponder including a receiver having a Schottky diode  
6 detector including a Schottky diode having a first terminal coupled to  
7 the antenna and having a second terminal; and means for driving  
8 current through both the antenna and the Schottky diode in a direction  
9 from the first terminal to the second terminal.

10 Another aspect of the invention provides a system comprising an  
11 antenna;

12 a transponder including a receiver having a Schottky diode detector  
13 including a Schottky diode having a first terminal coupled to the  
14 antenna and having a second terminal; and means for driving current  
15 through both the antenna and the Schottky diode in a direction from  
16 the second terminal to the first terminal. Another aspect of the  
17 invention provides a system comprising an antenna;

18 a transponder including a receiver having a Schottky diode detector  
19 including a Schottky diode having an anode coupled to the antenna and  
20 having a cathode; and means for driving current through both the  
21 antenna and the Schottky diode in a direction from the anode to the  
22 cathode.

23 Another aspect of the invention provides a radio frequency  
24 communications system comprising: an antenna; an integrated circuit

1 including a receiver having a Schottky diode detector including a  
 2 Schottky diode having an anode coupled to the antenna and having a  
 3 cathode, the Schottky diode detector further including a capacitor  
 4 connected between the cathode and ground, and including a capacitor  
 5 having a first contact connected to the cathode and having a second  
 6 contact defining an output of the Schottky diode detector; a current  
 7 source connected to the cathode to drive current through the antenna  
 8 and the Schottky diode in a direction from the anode to the cathode.

9 Another aspect of the invention provides a radio frequency  
 10 communications system comprising an antenna; an integrated circuit  
 11 including a receiver having a Schottky diode detector including a  
 12 Schottky diode having a cathode coupled to the antenna and having an  
 13 anode, the Schottky diode detector further including a capacitor  
 14 connected between the anode and ground, and including a capacitor  
 15 having a first contact connected to the anode and having a second  
 16 contact defining an output of the Schottky diode detector; and  
 17 a current source connected to the anode to drive current through the  
 18 antenna and the Schottky diode in a direction from the anode to the  
 19 cathode.

20 Another aspect of the invention provides a system comprising an  
 21 antenna; a transponder including a receiver having a Schottky diode  
 22 detector including a Schottky diode having a cathode coupled to the  
 23 antenna and having an anode; and means for driving current through  
 24



mirrors multiplying up the current of the current source, the frequency of oscillation of the frequency lock loop varying in response to selection of the current mirrors, the current mirrors including transistors operating in a subthreshold mode.

Another aspect of the invention provides a timing oscillator that consumes less than one milliAmp.

Another aspect of the invention provides a method of constructing a frequency lock loop including a current controlled oscillator having a plurality of selectively engageable current mirrors, the frequency of oscillation of the frequency lock loop varying in response to selection of the current mirrors, the method comprising selecting current mirrors to vary frequency of operation, and operating transistors in the current mirrors in subthreshold mode.

Another aspect of the invention provides a method of operating an integrated circuit including a receiver, a transmitter, and a frequency lock loop including a current source having a thermal voltage generator, a current controlled oscillator having a plurality of selectively engageable current mirrors multiplying up the current of the current source, the frequency of oscillation of the frequency lock loop varying in response to selection of the current mirrors, the method comprising engaging selected current mirrors and operating transistors in the current mirrors in a subthreshold mode.

Another aspect of the invention provides an amplifier powered by a selectively engageable voltage source, the amplifier comprising first and

second electrodes for receiving an input signal to be amplified, the input electrodes being adapted to be respectively connected to coupling capacitors; a differential amplifier having inputs respectively connected to the first and second electrodes, and having an output; selectively engageable resistances between the voltage source and respective inputs of the differential amplifier and defining, with the coupling capacitors, the high pass characteristics of the circuit; and second selectively engageable resistances between the voltage source and respective inputs of the differential amplifier, the second resistances respectively having smaller values than the first mentioned resistances, the second resistances being engaged then disengaged in response to the voltage source being engaged.

Another aspect of the invention provides a radio frequency identification device comprising an integrated circuit including a microprocessor, a receiver receiving radio frequency commands from an interrogation device, and a transmitter transmitting a signal identifying the device to the interrogator, the integrated circuit switching between a sleep mode, and a microprocessor on mode, in which more power is consumed than in the sleep mode, if the microprocessor determines that a signal received by the receiver is a radio frequency command from an interrogation device, the integrated circuit further including an amplifier powered by a selectively engageable voltage source engaged in the microprocessor on mode but not in the sleep mode, the amplifier including first and second electrodes for receiving an input signal to be

amplified, the input electrodes being adapted to be respectively connected to coupling capacitors, a differential amplifier having inputs respectively connected to the first and second electrodes, and having an output, selectively engageable resistances between the voltage source and respective inputs of the differential amplifier, second selectively engageable resistances between the voltage source and respective inputs of the differential amplifier, the second resistances respectively having smaller values than the first mentioned resistances, the second resistances being engaged then disengaged in response to the integrated circuit switching from the sleep mode to the microprocessor on mode. Another aspect of the invention provides a method of speeding power up of an amplifier stage powered by a selectively voltage source and including first and second electrodes for receiving an input signal to be amplified, the input electrodes being adapted to be respectively connected to coupling capacitors; a differential amplifier having inputs respectively connected to the first and second electrodes, and having an output; and selectively engageable resistances between the voltage source and respective inputs of the differential amplifier, the method comprising: shorting around the selectively engageable resistances for a predetermined amount of time in response to the voltage source being engaged.

Another aspect of the invention provides a radio frequency communications system comprising an antenna; an integrated circuit including a receiver having a Schottky diode detector including a

1 Schottky diode having an anode coupled to the antenna and having a  
2 cathode, the Schottky diode detector further including a capacitor  
3 connected between the cathode and ground, and including a capacitor  
4 having a first contact connected to the cathode and having a second  
5 contact defining an output of the Schottky diode detector, the integrated  
6 circuit further including a clock recovery circuit recovering a clock from  
7 rising edges only of a signal at the output of the Schottky diode  
8 detector; and a current source connected to drive current through the  
9 antenna and the Schottky diode in a direction from the anode to the  
10 cathode.

11 Another aspect of the invention provides a radio frequency  
12 communications system comprising an antenna; an integrated circuit  
13 including a receiver having a Schottky diode detector including a  
14 Schottky diode having a cathode coupled to the antenna and having an  
15 anode, the Schottky diode detector further including a capacitor  
16 connected between the anode and ground, and including a capacitor  
17 having a first contact connected to the anode and having a second  
18 contact defining an output of the Schottky diode detector, the integrated  
19 circuit further including a clock recovery circuit recovering a clock from  
20 falling edges only of a signal at the output of the Schottky diode  
21 detector; and a current source connected to drive current through the  
22 antenna and the Schottky diode in a direction from the anode to the  
23 cathode.



1 Another aspect of the invention provides a method of recovering  
2 a clock in a radio frequency communications system, the method  
3 comprising: providing an antenna; providing a receiver having a  
4 Schottky diode detector including a Schottky diode having an anode  
5 coupled to the antenna and having a cathode, the Schottky diode  
6 detector further including a capacitor connected between the cathode  
7 and ground, and including a capacitor having a first contact connected  
8 to the cathode and having a second contact defining an output of the  
9 Schottky diode detector; driving current through the antenna and the  
10 Schottky diode in a direction from the anode to the cathode; and  
11 recovering a clock from rising edges only of a signal at the output of  
12 the Schottky diode detector.

13 Another aspect of the invention provides a method of recovering  
14 a clock in a radio frequency communications system, the method  
15 comprising: providing an antenna; providing a receiver having a  
16 Schottky diode detector including a Schottky diode having a cathode  
17 coupled to the antenna and having an anode, the Schottky diode  
18 detector further including a capacitor connected between the anode and  
19 ground, and including a capacitor having a first contact connected to  
20 the anode and having a second contact defining an output of the  
21 Schottky diode detector; driving current through the antenna and the  
22 Schottky diode in a direction from the anode to the cathode; and  
23 recovering a clock from falling edges only of a signal at the output of  
24 the Schottky diode detector.

Another aspect of the invention provides a stage for a voltage controlled oscillator, the stage comprising a first transistor having a control electrode defining a first input, and having first and second power electrodes, the first power electrode defining a first node; a second transistor having a control electrode defining a second input, and having first and second power electrodes, the first power electrode of the second transistor defining a second node; a current source connected to the second power electrodes of the first and second transistors and directing current away from the second power electrodes of the first and second transistors; and means defining a variable resistance connecting the first and second nodes to a supply voltage.

Another aspect of the invention provides a stage for a voltage controlled oscillator, the stage comprising a first p-channel transistor having a gate defining a control node, having a source adapted to be connected to a supply voltage, and having a drain; a second p-channel transistor having a gate connected to the control node, having a source connected to the supply voltage, and having a drain; a first n-channel transistor having a gate defining a first input, having a drain connected to the drain of the first p-channel transistor and defining a first node, and having a source; a second n-channel transistor having a gate defining a second input, having a drain connected to the drain of the second p-channel transistor and defining a second node, and having a source; a current source connected to the sources of the first and second n-channel transistors directing current from the sources of the

first and second n-channel transistors; a first resistor connected between the supply voltage and the drain of the first n-type transistor; a second resistor connected between the supply voltage and drain of the second n-type transistor; a first source follower having an input connected to the first node and having an output defining a first output of the stage; and a second source follower having an input connected to the second node and having an output defining a second output of the stage.

Another aspect of the invention provides a transmitter including a ring oscillator having a chain of stages, each stage comprising a first p-channel transistor having a gate defining a control node, having a source adapted to be connected to a supply voltage, and having a drain; a second p-channel transistor having a gate connected to the control node, having a source connected to the supply voltage, and having a drain; a first n-channel transistor having a gate defining a first input, having a drain connected to the drain of the first p-channel transistor and defining a first node, and having a source; a second n-channel transistor having a gate defining a second input, having a drain connected to the drain of the second p-channel transistor and defining a second node, and having a source; a current source connected to the sources of the first and second n-channel transistors directing current from the sources of the first and second n-channel transistors; a first resistor connected between the supply voltage and the drain of the first n-type transistor; a second resistor connected between the supply voltage and drain of the second n-type transistor; a first

1 source follower having an input connected to the first node and having  
2 an output defining a first output of the stage; and a second source  
3 follower having an input connected to the second node and having an  
4 output defining a second output of the stage.

5 Another aspect of the invention provides a method of varying  
6 frequency in a stage of a voltage controlled oscillator having two input  
7 transistors having gates defining input nodes and having drain to source  
8 paths adapted to be connected between a supply voltage and a current  
9 source, the method comprising providing an impedance between the  
10 input transistors and the supply voltage, and varying the impedance.

11 Another aspect of the invention provides a frequency doubler  
12 comprising a first Gilbert cell; a second Gilbert cell coupled to the first  
13 Gilbert cell; a frequency generator configured to apply a first sinusoidal  
14 wave to the first Gilbert cell; and a phase shifter applying a sinusoidal  
15 wave shifted from the first sinusoidal wave to the second Gilbert cell.

16 Another aspect of the invention provides a frequency doubler  
17 comprising a first Gilbert cell including a first pair of transistors having  
18 sources that are connected together, a second pair of transistors having  
19 sources that are connected together, a first one of the transistors of the  
20 first pair having a gate defining a first input node and a first one of  
21 the transistors of the second pair having a gate connected to the first  
22 input node, a second one of the transistors of the first pair having a  
23 gate defining a second input node and a second one of the transistors  
24 of the second pair having a gate connected to the second input node,

the first transistor of the first pair having a drain, and the second transistor of the second pair having a drain connected to the drain of the first transistor of the first pair, the second transistor of the first pair having a drain, and the first transistor of the second pair having a drain connected to the drain of the second transistor of the first pair, a third pair including first and second transistors having sources coupled together, the first transistor of the third pair having a drain connected to the source of the second transistor of the first pair, the second transistor of the third pair having a drain connected to the source of the second transistor of the second pair, and a current source connected to the sources of the third pair and forward biasing the third pair, the second transistor of the third pair having a gate defining a third input node, and the first transistor of the third pair having a gate defining a fourth input node; and a second Gilbert cell including a first pair of transistors having sources that are connected together, a second pair of transistors having sources that are connected together, a first one of the transistors of the first pair of the second cell having a gate defining a first input node and a first one of the transistors of the second pair of the second cell having a gate connected to the first input node of the second cell, a second one of the transistors of the first pair of the second cell having a gate defining a second input node of the second cell and a second one of the transistors of the second pair of the second cell having a gate connected to the second input node of the second cell, the first transistor of the first pair of the



1 second input node of the first cell, and the fourth input node of the  
2 second cell being connected to the first input node of the first cell.

3 Another aspect of the invention provides a method of doubling  
4 frequency without using a feedback loop, the method comprising:  
5 providing a first Gilbert cell; providing a second Gilbert cell coupled to  
6 the first Gilbert cell; applying a first sinusoidal wave to the first Gilbert  
7 cell; and applying a sinusoidal wave shifted from the first sinusoidal  
8 wave to the second Gilbert cell.

9 Another aspect of the invention provides a pseudo random number  
10 generator comprising a linear feedback shift register switchably operable  
11 in a first mode, and in a second mode wherein the shift register  
12 consumes more power than in the first mode.

13 Another aspect of the invention provides a method of generating  
14 a pseudo random number, the method comprising providing a linear  
15 feedback shift register; providing an oscillator which generates clock  
16 signals used by the linear feedback shift register for shifting; and  
17 providing a first power level to the oscillator when a pseudo random  
18 number is required, and providing a second power level, lower than the  
19 first power level, to the oscillator at other times. Another aspect of  
20 the invention provides a method of generating a pseudo random  
21 number, the method comprising: providing a linear feedback shift  
22 register; providing an oscillator which generates clock signals used by  
23 the linear feedback shift register for shifting; and operating the  
24 oscillator at a first frequency in response to a request for a pseudo

1 random number, and operating the oscillator at a second frequency  
2 lower than the first frequency after the pseudo random number is  
3 generated.

4 Another aspect of the invention provides a system comprising a  
5 microprocessor operating at a frequency; a linear feedback shift register  
6 operable in a low power mode, wherein the shift register operates at  
7 a frequency below the frequency of the microprocessor, and a high  
8 power mode wherein the shift register consumes more power than in  
9 the low power mode, operates at the frequency of the microprocessor,  
10 and shifts data into the microprocessor.

11 Another aspect of the invention provides a radio frequency  
12 identification device comprising an integrated circuit including a receiver,  
13 a transmitter, a thermal voltage generator, a microprocessor operating  
14 at a frequency, a linear feedback shift register operable in a low power  
15 mode, wherein the shift register operates at a frequency below the  
16 frequency of the microprocessor, and a high power mode wherein the  
17 shift register consumes more power than in the low power mode,  
18 operates at the frequency of the microprocessor, and shifts data into the  
19 microprocessor, an oscillator supplying clock signals to the shift register,  
20 and current mirrors supplying current to each stage of the shift register,  
21 the current mirrors being referenced to the thermal voltage generator  
22 when the shift register is in the low power mode, and, when the shift  
23 register is in the high power mode, connected to a supply voltage  
24



1 potential greater than the potential provided by the thermal voltage  
2 generator.

3 Another aspect of the invention provides a method of generating  
4 a pseudo random number, the method comprising: providing a thermal  
5 voltage generator, a linear feedback shift register, an oscillator supplying  
6 clock signals to the shift register, and current mirrors supplying current  
7 to each stage of the shift register; referencing the current mirrors to  
8 the thermal voltage generator when no pseudo random number is  
9 required; and connecting the current mirrors to a supply voltage  
10 potential greater than the potential provided by the thermal voltage  
11 generator when a pseudo random number is required.

12 Another aspect of the invention provides an integrated circuit  
13 comprising a receiver and a transmitter sharing a common antenna.

14 Another aspect of the invention provides a method of using an  
15 integrated circuit including a receiver and a transmitter, the method  
16 comprising connecting the receiver and transmitter to a common  
17 antenna.

18 Another aspect of the invention provides an integrated circuit  
19 comprising:

20 a die including a transmitter having an antenna output and a detector  
21 having an antenna input; a package housing the die; a first contact  
22 connected to the antenna output and accessible from outside the  
23 package; a second contact connected to the antenna input and accessible  
24

1 from outside the package; and a short electrically connecting the first  
2 contact to the second contact outside the package.

3 Another aspect of the invention provides a method of using an  
4 integrated circuit including a die having a transmitter including an  
5 antenna output and a detector including an antenna output, the  
6 integrated circuit further including a package housing the die, a first  
7 contact connected to the antenna output and accessible from outside the  
8 package, and a second contact connected to the antenna input and  
9 accessible from outside the package, the method comprising: electrically  
10 shorting the first contact to the second contact outside the package.

11 Another aspect of the invention provides a transceiver comprising  
12 an antenna having a first end connected to a bias voltage, and having  
13 a second end; a detector including a Schottky diode having an anode  
14 connected to the second end of the antenna; and a transmitter having  
15 an output connected to the second end of the antenna.

16 Another aspect of the invention provides a radio frequency  
17 identification device comprising an integrated circuit including both a  
18 receiver and a transmitter; a first antenna connected to the receiver;  
19 and a second antenna connected to the transmitter.

20 Another aspect of the invention provides a transceiver comprising  
21 a loop antenna having a first end connected to a bias voltage, and  
22 having a second end; a second antenna; a detector including a Schottky  
23 diode having an anode connected to the second end of the antenna;  
24 and a transmitter having an output connected to the second antenna.

1 Another aspect of the invention provides a transceiver comprising  
2 an antenna having a first end connected to a bias voltage, and having  
3 a second end; a detector including a Schottky diode having an anode  
4 connected to the second end of the antenna; and an active transmitter  
5 having an output connected to the second end of the antenna.

6 Another aspect of the invention provides a transceiver comprising  
7 an antenna having a first end, and having a second end; a detector  
8 including a Schottky diode having a cathode connected to the second  
9 end of the antenna and defining a potential at the second end of the  
10 antenna, the first end of the antenna being connected to a potential  
11 lower than the potential of the second end of the antenna; and a  
12 backscatter transmitter including a transistor having a first power  
13 electrode connected to the first end of the antenna, a second power  
14 electrode connected to the second end of the antenna, and a control  
15 electrode adapted to have a modulation signal applied thereto.

16 Another aspect of the invention provides a transceiver in  
17 accordance with claim and further comprising a current source directing  
18 current in the direction from the anode to the cathode.

19 Another aspect of the invention provides a transceiver comprising  
20 a loop antenna having a first end connected to a bias voltage, and  
21 having a second end; a detector including a Schottky diode having an  
22 anode connected to the second end of the antenna; a backscatter  
23 transmitter having a first output and having a second output; a  
24 capacitor connected between the first output and the first end of the

1 antenna; and a capacitor connected between the second output and the  
2 second end of the antenna.

3 Another aspect of the invention provides a method of configuring  
4 a transceiver including a backscatter transmitter having first and second  
5 outputs, and a detector having a Schottky diode including an anode, the  
6 method comprising: applying a bias voltage to a first end of an  
7 antenna; connecting a second end of the antenna to the anode;  
8 connecting a capacitor between the first output and the first end of the  
9 antenna; and connecting a capacitor between the second output and the  
10 second end of the antenna.

11 Another aspect of the invention provides a method of arranging  
12 a transceiver including a backscatter transmitter and a detector having  
13 a Schottky diode including a cathode, the method comprising:  
14 connecting a first end of an antenna to a ground potential; connecting  
15 a second end of the antenna to the cathode; and connecting a first  
16 power electrode of a transistor to the first end of the antenna;  
17 connecting a second power electrode connected to the second end of  
18 the antenna; and connecting a control electrode of the transistor to a  
19 modulation signal.

20 Another aspect of the invention provides a method of determining  
21 when a phase lock loop achieves frequency lock relative to a desired  
22 frequency, the phase lock loop including a voltage controlled oscillator  
23 having a control node and oscillating at a frequency responsive to the  
24 voltage applied to the control node, the method comprising: crossing

1 the voltage that would result in the phase lock loop tracking the  
2 desired frequency in a first direction; crossing the voltage that would  
3 result in the phase lock loop tracking the desired frequency in a second  
4 direction opposite the first direction; and indicating that frequency lock  
5 has been achieved.

6 Another aspect of the invention provides a method of determining  
7 when frequency lock occurs relative to a desired frequency, the method  
8 comprising:

9 providing a phase lock loop including a voltage controlled oscillator that  
10 oscillates at a frequency responsive to voltage applied to the voltage  
11 controlled oscillator; applying a voltage to the voltage controlled  
12 oscillator to produce a frequency of oscillation less than the desired  
13 frequency; increasing the voltage applied to the voltage controlled  
14 oscillator using one or more steps of a first size; increasing the voltage  
15 applied to the voltage controlled oscillator using one or more steps of  
16 a second size smaller than the first size; decreasing the voltage applied  
17 to the voltage controlled oscillator using one or more steps of a third  
18 size smaller than the second size; increasing the voltage applied to the  
19 voltage controlled oscillator using a step of the third size; and indicating  
20 that lock has occurred in response to the increase of the step of the  
21 third size.

22 Another aspect of the invention provides a method of determining  
23 when a phase lock loop achieves frequency lock relative to a desired  
24 frequency, the phase lock loop including a voltage controlled oscillator

1 having a control node and oscillating at a frequency responsive to the  
2 voltage applied to the control node, the method comprising: increasing  
3 the voltage applied to the control node to a voltage above the voltage  
4 that would result in the phase lock loop tracking the desired frequency;  
5 decreasing the voltage applied to the control node to a voltage below  
6 the voltage that would result in the phase lock loop tracking the  
7 desired frequency; and increasing the voltage applied to the control  
8 node and indicating that frequency lock has been achieved.

9 Another aspect of the invention provides a radio frequency  
10 identification device comprising an integrated circuit including a  
11 microprocessor, a transmitter, and a receiver, the integrated circuit  
12 periodically switching between a sleep mode, and a receiver-on mode in  
13 which more power is consumed than in the sleep mode, and further  
14 including a selectively engageable timer preventing switching from the  
15 sleep mode to the receiver-on mode for a predetermined amount of  
16 time.

17 Another aspect of the invention provides a radio frequency  
18 identification device comprising an integrated circuit including a  
19 microprocessor, a transmitter, and a receiver, the integrated circuit  
20 periodically switching between a sleep mode, and a receiver-on mode in  
21 which more power is consumed than in the sleep mode, and further  
22 including means for selectively preventing switching from the sleep mode  
23 to the receiver-on mode for a predetermined amount of time.

Another aspect of the invention provides a radio frequency identification device comprising an integrated circuit including a microprocessor, a transmitter, and a receiver, the integrated circuit being switchable between a sleep mode, and a mode in which more power is consumed than in the sleep mode, the integrated circuit being switched from the sleep mode to the mode in which more power is consumed in response to a direct sequence spread spectrum modulated radio frequency signal being received by the receiver which has a predetermined number of transitions within a certain period of time, the integrated circuit further including a selectively engageable timer which prevents switching from the sleep mode for a period of time regardless of whether a signal is subsequently received by the receiver which has the predetermined number of transitions within a certain period of time.

Another aspect of the invention provides a method for conserving power in a radio frequency identification device, the method comprising: periodically switching from a sleep mode to a receiver on mode and performing tests to determine whether to further switch to a microprocessor on mode because a valid radio frequency signal is present; and selectively disabling the periodic switching from the sleep mode for a predetermined amount of time.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

1 This disclosure of the invention is submitted in furtherance of the  
2 constitutional purposes of the U.S. Patent Laws "to promote the  
3 progress of science and useful arts" (Article 1, Section 8).

#### 4 5 Overview of Device

6 Fig. 1 illustrates a radio frequency data communication device 12  
7 embodying the invention. The radio frequency data communication  
8 device 12 includes an integrated circuit 16, a power source 18 connected  
9 to the integrated circuit 16 to supply power to the integrated circuit 16,  
10 and at least one antenna 14 connected to the integrated circuit 16 for  
11 radio frequency transmission and reception by the integrated circuit 16.  
12 For purposes of this disclosure, including the appended claims, the term  
13 "integrated circuit" shall be defined as a combination of interconnected  
14 circuit elements inseparably associated on or within a continuous  
15 substrate. For purposes of this disclosure, including the appended  
16 claims, the term "semiconductive substrate" is defined to mean any  
17 construction comprising semiconductive material, including, but not limited  
18 to, bulk semiconductive materials such as a semiconductive wafer (either  
19 alone or in assemblies comprising other materials thereon), and  
20 semiconductive material layers (either alone or in assemblies comprising  
21 other materials). For purposes of this disclosure, including the  
22 appended claims, the term "substrate" refers to any supporting structure,  
23 including, but not limited to, the semiconductive substrates described  
24 above. In the illustrated embodiment, the integrated circuit 16 is a



1 monolithic integrated circuit. For purposes of this disclosure, including  
2 the appended claims, the term "monolithic integrated circuit" shall be  
3 defined as an integrated circuit wherein all circuit components are  
4 manufactured into or on top of a single chip of silicon. The integrated  
5 circuit 16 will be described in greater detail below. The power  
6 source 18 is a battery or other suitable power source.

### 7 8 Housing

9 The radio frequency data communication device 12 can be  
10 included in any appropriate housing or packaging.

11 Fig. 2 shows but one example in the form of an employee  
12 identification badge 10 including the radio frequency data communication  
13 device 12, and a card 11 made of plastic or other suitable material.  
14 In one embodiment, the radio frequency data communication device 12  
15 is laminated to the back face of the plastic card 11, and the card  
16 forms the visible portion of the badge. In another embodiment, the  
17 radio frequency data communication device 12 is bonded to the back  
18 face of the card by embedding it within a thin bond line of epoxy-  
19 based material. Alternatively, the radio frequency data communication  
20 device 12 is embedded into the plastic card 11. In one embodiment,  
21 the front face of the badge 10 has visual identification features  
22 including an employee photograph as well as identifying text.

23 Fig. 3 illustrates but one alternative housing supporting the  
24 device 12. More particularly, Fig. 3 shows a miniature housing 20

1 encasing the device 12 to define a tag which can be supported by an  
2 object (e.g., hung from an object, affixed to an object, etc.). The  
3 housing 20 preferably has the general shape and size, in plan view, of  
4 a postage stamp. The embodiment of Fig. 3 also includes a card 21  
5 supporting the device 12 in the housing 20. The card 21 is formed of  
6 plastic or other suitable material having a thickness of about 0.040  
7 inches, a width of about 1.25 inches, and a height of about 1.25 inches.  
8 In one embodiment, the device 12 is bonded to a back face of the  
9 card 21 with a thin layer of non-conductive epoxy material that  
10 cooperates with the card to define the housing 20.

11 Although two particular types of housings have been disclosed, the  
12 device 12 can be included in any appropriate housing. The device 12  
13 is of a small size that lends itself to applications employing small  
14 housings, such as cards, miniature tags, etc. Larger housings can also  
15 be employed. The device 12, housed in any appropriate housing, can  
16 be supported from or attached to an object in any desired manner; for  
17 example using double sided tape, glue, lanyards, leash, nails, staples,  
18 rivets, or any other fastener. The housing can be sewn on to an  
19 object, hung from an object, implanted in an object (hidden), etc.

## 20 21 Antenna

22 Various configurations are possible for the antenna 14. The  
23 integrated circuit 16 includes a receiver 30 and a transmitter 32  
24 (Fig. 5). In one embodiment, separate antennas 44 and 46 are

1 provided for receiver and transmitter of the integrated circuit 16. In  
2 another embodiment (Fig. 1), a single antenna is shared by the receiver  
3 and transmitter sections. In one embodiment, the antenna is defined  
4 by conductive epoxy screened onto a card or housing. In the illustrated  
5 embodiment, the antenna is conductively bonded to the integrated circuit  
6 via bonding pads.

7 In an embodiment where a single antenna is employed, that single  
8 antenna preferably comprises a folded dipole antenna defining a  
9 continuous conductive path, or loop, of microstrip. Alternatively, the  
10 antenna can be constructed as a continuous loop antenna.

#### 11 Battery

12 ~~Sub~~ ~~B2~~ ~~As~~ 13 If the power source 18 is a battery, the battery can take any  
14 suitable form. Preferably, the battery type will be selected depending  
15 on weight, size, and life requirements for a particular application. In  
16 one embodiment, the battery 18 is a thin profile button-type cell  
17 forming a small, thin energy cell more commonly utilized in watches and  
18 small electronic devices requiring a thin profile. A conventional button-  
19 type cell has a pair of electrodes, an anode formed by one face and  
20 a cathode formed by an opposite face. Exemplary button-type cells are  
21 disclosed in several pending U.S. patent applications including U.S.  
22 Patent Application Serial No. 08/205,957, "Button-Type Battery Having  
23 Bendable Construction and Angled Button-Type Battery," listing Mark E.  
24 Tuttle and Peter M. Blonsky as inventors; U.S. Patent Application Serial

1 No. 08/321,251, "Button-Type Batteries and Method of Forming Button-  
2 Type Batteries," listing Mark E. Tuttle as inventor; and U.S. Patent  
3 Application Serial No. 08/348,543, "Method of Forming Button-Type  
4 Batteries and a Button-Type Battery Insulating and Sealing Gasket,"  
5 listing Mark E. Tuttle as inventor. These patent applications and  
6 resulting patents are hereby incorporated by reference. In an  
7 alternative embodiment, the battery 18 comprises a series connected pair  
8 of button type cells. Instead of using a battery, any suitable power  
9 source can be employed.

#### 10 11 Overview of Communication System

12 Fig. 4 illustrates a radio frequency communication system 24  
13 including the device 12 and a radio frequency interrogator unit  
14 (hereinafter "interrogator") 26. The device 12 transmits and receives  
15 radio frequency communications to and from the interrogator 26.  
16 Preferably, the interrogator unit 26 includes an antenna 28, as well as  
17 dedicated transmitting and receiving circuitry, similar to that implemented  
18 on the integrated circuit 16. The system 24 further includes a host  
19 computer 48 in communication with the interrogator 26. The host  
20 computer 48 acts as a master in a master-slave relationship with the  
21 interrogator 26. The host computer 48 includes an applications program  
22 for controlling the interrogator 26 and interpreting responses, and a  
23 library ("MRL") of radio frequency identification device applications or  
24 functions. Most of the functions communicate with the interrogator 26.

1 These functions effect radio frequency communication between the  
2 interrogator 26 and the device 12. These functions are described below  
3 in a section titled "Protocol."

4 One example of an interrogator implemented in combination with  
5 a transponder unit is disclosed in U.S. Patent No. 4,857,893, hereby  
6 incorporated by reference. Generally, the interrogator 26 includes an  
7 antenna 28, and transmits an interrogation signal or command 27  
8 ("forward link") via the antenna 28. The device 12 receives the  
9 incoming interrogation signal via its antenna 14. Upon receiving the  
10 signal 27, the device 12 responds by generating and transmitting a  
11 responsive signal or reply 29 ("return link"). Preferably, the responsive  
12 signal 29 is encoded with information that uniquely identifies, or labels  
13 the particular device 12 that is transmitting, so as to identify any object  
14 or person with which the device 12 is associated.

15 In the illustrated embodiment in Fig. 4, there is no communication  
16 between devices 12. Instead, the devices 12 communicate with the  
17 interrogator 26. Fig. 4 illustrates the device 12 as being in the  
18 housing 20 of Fig. 3. The system 24 would operate in a similar  
19 manner if the device 12 is provided in a housing such as the  
20 housing 10 of Fig. 2, or any other appropriate housing. Multiple  
21 devices 12 can be used in the same field of an interrogator 26 (i.e.,  
22 within communications range of an interrogator 26). Similarly, multiple  
23 interrogators 26 can be in proximity to one or more of the devices 12.

Sub 14  
B3

Various U.S. patent applications, which are incorporated herein by reference, disclose features that are employed in various alternative embodiments of the invention: 08/092,147, filed July 15, 1993, "Wake Up Device for a Communications System" and continuation application 08/424,827, filed April 19, 1995, "Wake Up Device for a Communications System"; 08/281,384, filed July 27, 1994, "Communication System Having Transmitter Frequency Control"; 07/990,918, filed December 15, 1992, now U.S. Patent No. 5,365,551, "Data Communication Transceiver Using Identification Protocol"; 07/899,777, filed June 17, 1992, "Radio Frequency Identification Device (RFID) and Method of Manufacture, Including an Electrical Operating System and Method," now abandoned; 07/921,037, filed July 24, 1992, "Anti-Theft Method for Detecting The Unauthorized Opening of Containers and Baggage," now abandoned; 07/928,899, filed August 12, 1992, "Electrically Powered Postage Stamp or Mailing or Shipping Label Operative with Radio Frequency (RF) Communications," now abandoned; and 08/032,384, filed on March 17, 1993, "Modulated Spread Spectrum in RF Identification Systems Method," now allowed.

The above described system 24 is advantageous over prior art devices that utilize magnetic field effect systems because, with the system 24, a greater range can be achieved, and more information can be obtained (instead of just an identification number).

As a result, such a system 24 can be used, for example, to monitor large warehouse inventories having many unique products

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1 needing individual discrimination to determine the presence of particular  
2 items within a large lot of tagged products. The system can also be  
3 used to counteract terrorism to monitor luggage entering a plane to  
4 ensure that each item of luggage that enters the plane is owned by a  
5 passenger who actually boards the plane. Such a technique assumes  
6 that a terrorist will not board a plane that he or she is planning to  
7 bomb. The system 24 is useful whenever RF transmission over a large  
8 range is desirable, such as for inventory control. In one embodiment,  
9 the sensitivity of the devices 12 is adjustable so that only devices within  
10 a certain range of the interrogator 26 will respond. In another  
11 embodiment, the power of the interrogator 26 is adjustable so that only  
12 devices within a certain range of the interrogator 26 will respond.

13 However, a power conservation problem is posed by such  
14 implementations where batteries are used to supply power to the  
15 integrated circuits 16. If the integrated circuit 16 operates continuously  
16 at full power, battery life will be short, and device 12 will have to be  
17 frequently replaced. If the battery 18 is permanently sealed in a  
18 housing, replacement of the battery will be difficult or impossible. For  
19 example, one reason for sealing the battery with the integrated circuit  
20 16 and antenna 14 in a housing is to simplify the design and  
21 construction, to reduce the cost of production, and protect the electrical  
22 interconnections between devices. Another reason is protection of the  
23 battery and integrated circuit 16 from moisture and contaminants. A  
24 third reason is to enhance the cosmetic appeal of the device 12 by

eliminating the need for an access port or door otherwise necessary to insert and remove the battery. When the battery is discharged, the entire badge or stamp is then discarded. It is therefore desirable in this and other applications to incorporate power conservation techniques into the integrated circuit 16 in order to extend useful life.

In one embodiment, the devices 12 switch between a "sleep" mode of operation, and higher power modes to conserve energy and extend battery life during periods of time where no interrogation signal 27 is received by the device 12. These power conservation techniques are described in greater detail below.

In one embodiment of the invention, in order to further extend the life of the battery 18, the receiver sensitivity of the device 12 is tuned over a range of tuned and detuned states in order to modify the ability of the device to detect signal 27, and therefore adjust the tendency for the device to wake up. One way to adjust the receiver sensitivity is by adjusting the sensitivity, or impedance of the antenna. Another way is by controlling the gain of amplifiers included in the receiver. Another way is to adjust or switch in different circuit elements in the device 12, thereby realizing different circuit configurations. Additionally, the transmitting sensitivity for the device 12 can be adjusted. For example, transmitting range can be adjusted by controlling interrogator continuous wave power if the transmitter is operating in backscatter mode, and by controlling output power if the transmitter is in active mode.



1 Overview of Integrated Circuit

2 Fig. 5 is a high level circuit schematic of the integrated circuit 16  
3 utilized in the devices of Figs. 1-4. In the embodiment shown in  
4 Fig. 5, the integrated circuit 16 is a monolithic integrated circuit. More  
5 particularly, in the illustrated embodiment, the integrated circuit 16  
6 comprises a single die, having a size of 209 x 116 mils<sup>2</sup>, including the  
7 receiver 30, the transmitter 32, a micro controller or microprocessor 34,  
8 a wake up timer and logic circuit 36, a clock recovery and data  
9 recovery circuit 38, and a bias voltage and current generator 42.

10 In one embodiment, a spread spectrum processing circuit 40 is  
11 also included in the integrated circuit 16 and formed relative to the  
12 single die. In this embodiment, signals received by the receiver 30 are  
13 modulated spread spectrum signals. Spread spectrum modulation is  
14 described below. In the illustrated embodiment, the modulation scheme  
15 for replies sent by the transmitter 32 is selectable. One of the  
16 available selections for replies sent by the transmitter 32 is modulated  
17 spread spectrum.

18  
19 Spread Spectrum Modulation

20 Many modulation techniques minimize required transmission  
21 bandwidth. However, the spread spectrum modulation technique  
22 employed in the illustrated embodiment requires a transmission  
23 bandwidth that is up to several orders of magnitude greater than the  
24 minimum required signal bandwidth. Although spread spectrum

1 modulation techniques are bandwidth inefficient in single user  
 2 applications, they are advantageous where there are multiple users, as  
 3 is the case with the instant radio frequency identification system 24.  
 4 The spread spectrum modulation technique of the illustrated embodiment  
 5 is advantageous because the interrogator signal can be distinguished from  
 6 other signals (e.g., radar, microwave ovens, etc.) operating at the same  
 7 frequency. The spread spectrum signals transmitted by the device 12  
 8 and by the interrogator 26 (Fig. 4) are pseudo random and have  
 9 noise-like properties when compared with the digital command or reply.  
 10 The spreading waveform is controlled by a pseudo-noise or pseudo  
 11 random number (PN) sequence or code (described below). The PN  
 12 code is a binary sequence that appears random but can be reproduced  
 13 in a predetermined manner by the device 12. More particularly,  
 14 incoming spread spectrum signals are demodulated by the device 12  
 15 through cross correlation with a version of the pseudo random carrier  
 16 that is generated by the device 12 itself. Cross correlation with the  
 17 correct PN sequence unspreads the spread spectrum signal and restores  
 18 the modulated message in the same narrow band as the original data.

19 A pseudo-noise or pseudo random sequence (PN sequence) is a  
 20 binary sequence with an autocorrelation that resembles, over a period,  
 21 the autocorrelation of a random binary sequence. The autocorrelation  
 22 of a pseudo-noise sequence also roughly resembles the autocorrelation  
 23 of band-limited white noise. A pseudo-noise sequence has many  
 24 characteristics that are similar to those of random binary sequences.

1 For example, a pseudo-noise sequence has a nearly equal number of  
2 zeros and ones, very low correlation between shifted versions of the  
3 sequence, and very low cross correlation between any two sequences.  
4 A pseudo-noise sequence is usually generated using sequential logic  
5 circuits. For example, a pseudo-noise sequence can be generated using  
6 a feedback shift register.

7 A feedback shift register comprises consecutive stages of two state  
8 memory devices, and feedback logic. Binary sequences are shifted  
9 through the shift registers in response to clock pulses, and the output  
10 of the various stages are logically combined and fed back as the input  
11 to the first stage. The initial contents of the memory stages and the  
12 feedback logic circuit determine the successive contents of the memory.

13 The illustrated embodiment employs direct sequence spread  
14 spectrum modulation. A direct sequence spread spectrum (DSSS) system  
15 spreads the baseband data by directly multiplying the baseband data  
16 pulses with a pseudo-noise sequence that is produced by a pseudo-noise  
17 generator. A single pulse or symbol of the PN waveform is called a  
18 "chip." Synchronized data symbols, which may be information bits or  
19 binary channel code symbols, are added in modulo-2 fashion to the  
20 chips before being modulated. The receiver performs demodulation.  
21 For example, in one embodiment the data is phase modulated, and the  
22 receiver performs coherent or differentially coherent phase-shift keying  
23 (PSK) demodulation. In another embodiment, the data is amplitude  
24 modulated. Assuming that code synchronization has been achieved at

1 the receiver, the received signal passes through a wideband filter and  
2 is multiplied by a local replica of the PN code sequence. This  
3 multiplication yields the unspread signal.

4 A pseudo-noise sequence is usually an odd number of chips long.  
5 In the illustrated embodiment, one bit of data is represented by a  
6 thirty-one chip sequence. A zero bit of data is represented by inverting  
7 the pseudo-noise sequence.

8 Spread spectrum techniques are also disclosed in the following  
9 patent applications and patent, which are incorporated herein by  
10 reference: U.S. Patent Application Serial No. 08/092,147; U.S. Patent  
11 Application Serial No. 08/424,827, filed April 19, 1995; and U.S. Patent  
12 No. 5,121,407 to Partyka et al. They are also disclosed, for example,  
13 in "Spread Spectrum Systems," by R.C. Dixon, published by John Wiley  
14 and Sons, Inc.

15 The system disclosed in U.S. Patent Application Serial No.  
16 08/092,147 includes two receivers, a low power receiver for detecting a  
17 wake up signal from an interrogator, and a high power receiver for  
18 receiving commands from an interrogator. On the other hand, the  
19 integrated circuit 16 of the illustrated embodiment employs a single  
20 receiver for both wake up and receiving commands from an interrogator.  
21 Another difference is that in the system 12 of the illustrated  
22 embodiment the receiver, not the interrogator, controls wake up. In the  
23 system 24 of the illustrated embodiment, the integrated circuit 16  
24

1 includes a timer that causes the receiver and support circuitry to be  
2 powered on periodically. This is described in greater detail elsewhere.

### 3 4 Backscatter and Frequency Hopping

5 The interrogator sends out a command that is spread around a  
6 certain center frequency (e.g. 2.44 GHz). After the interrogator  
7 transmits the command, and is expecting a response, the interrogator  
8 switches to a CW mode (continuous wave mode). In the continuous  
9 wave mode, the interrogator does not transmit any information.  
10 Instead, the interrogator just transmits 2.44 GHz radiation. In other  
11 words, the signal transmitted by the interrogator is not modulated.  
12 After the device 12 receives the command from the interrogator, the  
13 device 12 processes the command. If the device 12 is in a backscatter  
14 mode it alternately reflects or does not reflect the signal from the  
15 interrogator to send its reply. For example, in the illustrated  
16 embodiment, two halves of a dipole antenna are either shorted together  
17 or isolated from each other, as described below in greater detail. In  
18 the illustrated embodiment, frequency hopping does not occur when the  
19 interrogator transmits a command, but occurs when the interrogator is  
20 in the continuous wave mode. The interrogator, in the continuous wave  
21 mode, hops between various frequencies close to the 2.44 GHz  
22 frequency. These various frequencies are sufficiently close to the 2.44  
23 GHz frequency that backscatter antenna reflection characteristics of the  
24 device 12 are not appreciably altered. Because the interrogator is

1 hopping between frequencies, the interrogator knows what frequency  
2 backscatter reflections to expect back from the device 12. By hopping  
3 between various frequencies, the amount of time the interrogator  
4 continuously uses a single frequency is reduced. This is advantageous  
5 in view of FCC regulatory requirements.

6 In the illustrated embodiment, no attempt is made to frequency  
7 hop at the interrogator to a pseudo-random sequence and then correlate  
8 to that at the receiver. However, in alternative embodiments, such  
9 correlation takes place.

#### 10 11 CMOS Process

12 The integrated circuit 16 is formed according to semiconductor  
13 wafer processing steps, such as CMOS semiconductor wafer processing  
14 steps used to form static random access memories. In the preferred  
15 embodiment, the integrated circuit 16 is a single metal integrated circuit.  
16 In other words, the integrated circuit 16 is formed using a single metal  
17 layer processing method. More particularly, only one layer of metal  
18 (e.g., aluminum) is employed. This is advantageous in that it results  
19 in a lower cost of production.

20 In this processing method, a p-type wafer is employed. The  
21 processing method employed provides n-well areas used to define  
22 p-channel transistors; an active area which is used to define p+ and n+  
23 diffused regions inside the p-type wafer or inside the n-well areas.  
24 Next, a layer is provided that helps prevent leakage between adjacent

1 devices. Then, transistor are defined by forming n-type and p-type  
2 polysilicon. Then, a contact layer is defined for connecting desired  
3 intersections of polysilicon with metal (aluminum) that is subsequently  
4 formed. The contact layer is also used, in some instances, for  
5 connecting desired intersections of the metal that is subsequently formed  
6 with active area. Then the metal layer is formed. The contact layer  
7 provides a means for connecting metal with layers below the metal.  
8 Then, a passivation step is performed. Passivation means that the die  
9 is covered with a protective layer and holes are cut around the edge  
10 of the die so that electrical connection can be made to the bond pads.

11 In some processing, after the metal layer is formed, an insulating  
12 layer is provided, and another layer of aluminum is formed above the  
13 insulating layer. Holes are provided at selected locations to  
14 interconnect the top layer of aluminum with lower layers. An  
15 advantage of using multiple layers of metal is that it provides greater  
16 flexibility in how functional blocks are laid out and in how power is  
17 bused to various areas. However, multiple metal layers add processing  
18 steps. This results in added cost and complexity.

19 The process of the preferred embodiment employs only one layer  
20 of metal, and is therefore a relatively simple, inexpensive process.

21 The following U.S. patents, which are incorporated herein by  
22 reference, disclose CMOS processing techniques that are employed in  
23 various alternative embodiments of the invention: 5,489,546 to Ahmad  
24 et al.; 5,272,367 to Dennison et al.; and 5,134,085 to Gilgen et al.

1 Various other processing methods can be employed in alternative  
2 embodiments.

### 3 4 Transmitter and Receiver

5 The receiver 30 is a radio frequency receiver included in the  
6 integrated circuit 16, and the transmitter 32 is a radio frequency  
7 transmitter included in the integrated circuit 16. In one embodiment,  
8 the receiver 30 includes a Schottky diode detector. Various forms of  
9 Schottky diode detectors are described in a paper titled "Designing  
10 Detectors for RF/ID Tags," by Raymond W. Waugh of Hewlett-Packard  
11 Company, submitted for presentation at the RF Expo, San Diego,  
12 February 1, 1995, and incorporated herein by reference.

13 The receiver 30 of the illustrated embodiment makes use of the  
14 rate or frequency of data included in incoming signals, but does not  
15 make use of the carrier frequency of the incoming signal. In other  
16 words, operation of the receiver 30 is independent of the frequency of  
17 the carrier of the incoming signal over a wide range of carrier  
18 frequencies.

19 Therefore, the device 12 can operate over a wide range of carrier  
20 frequencies. For example, the device 12 can operate with carriers of  
21 915-5800 MHZ. In a more particular embodiment, the device 12 can  
22 operate with carrier frequencies in the 915, 2450, or 5800 MHZ bands.  
23 In the illustrated embodiment, the antennas are half wave antennas, and  
24 frequency selectivity of the device 12 is achieved based on selection of



1 the antenna external to the integrated circuit 16. Capacitors employed  
2 in the Schottky diode detector are also selected based on the carrier  
3 frequency that will be employed.

4 In one embodiment, the transmitter 32 is switchable between  
5 operating in a modulated backscatter transmitter mode, and operating  
6 in an active mode. The transmitter 32 switches between the backscatter  
7 mode and the active mode in response to a radio frequency command,  
8 instructing the transmitter to switch, sent by the interrogator 26 and  
9 received by the receiver 30. In the active mode, a carrier for the  
10 transmitter is extracted from a signal received by the receiver 30.

11 Active transmitters are known in the art. See, for example, U.S.  
12 Patent Application Serial No. 08/281,384. U.S. Patent Application Serial  
13 No. 08/281,384 also discloses how transmit frequency for the transmitter  
14 32 is recovered from a message received via radio frequency from the  
15 interrogator 26. The device 12 differs from the device disclosed in U.S.  
16 Patent Application Serial No. 08/281,384 in that a VCO control voltage  
17 is stored as an analog voltage level on a capacitor instead of as a  
18 digital number in a register. Further, in the illustrated embodiment, the  
19 recovered frequency is also used by the integrated circuit 16 to generate  
20 a DPSK subcarrier for modulated backscatter transmission.

21 The transmitter is capable of transmitting using different  
22 modulation schemes, and the modulation scheme is selectable by the  
23 interrogator. More particularly, if it is desired to change the  
24 modulation scheme, the interrogator sends an appropriate command via

1 radio frequency. The transmitter can switch between multiple available  
2 modulation schemes such as Binary Phase Shift Keying (BPSK), Direct  
3 Sequence Spread Spectrum, On-Off Keying (OOK), and Modulated  
4 Backscatter (MBS).

#### 6 Wake Up Timer and Logic Circuit

7 The integrated circuit 16 includes the wake up timer and logic  
8 circuit 36 for conserving battery power. More particularly, the  
9 integrated circuit 16 normally operates in a sleep mode wherein most  
10 circuitry is inactive and there is a very low current draw on the  
11 battery 18. One circuit that is active during the sleep mode is a timer  
12 for waking up the integrated circuit at predetermined intervals. In the  
13 illustrated embodiment, the interval is 16 milliseconds; however, various  
14 other intervals can be selected by radio frequency by sending a message  
15 from the interrogator 26 to the device 12. For example, in the  
16 illustrated embodiment, the interval is selectable as being 0.5, 16, 64 or  
17 256 milliseconds.

18 Assuming the selected interval is 16 milliseconds, after every sleep  
19 period of 16 milliseconds the wake up timer and logic  
20 circuit 36 activates the receiver 30, the clock recovery and data recovery  
21 circuit 38, and all the bias currents and voltages associated with the  
22 receiver 30. This is a receiver on mode, illustrated by a vertical line  
23 marked WAKEUP RX ON in Fig. 27. Such bias currents and voltages  
24



1 If a radio frequency signal is detected upon wake up, the wake  
2 up timer and logic compares the incoming signal to known  
3 characteristics of expected spread spectrum encoded data. In the  
4 illustrated embodiment, a valid incoming radio frequency signal will be  
5 a spread spectrum signal having a thirty-one chip code representing a  
6 single data bit. To represent a digital one ("1") the thirty-one chip  
7 code is sent as is. To represent a digital zero ("0") the thirty-one chip  
8 code is inverted. The wake up timer and logic circuit 36 knows how  
9 many transitions there are in a valid thirty-one chip sequence, and  
10 knows the time period within which all those transitions are expected  
11 (or the frequency of the transitions). After the incoming radio  
12 frequency signal is amplified and converted to baseband, it is tested  
13 against known characteristics of a valid signal.

14 If the incoming signal does not pass these tests, the integrated  
15 circuit 16 returns to the sleep mode. If the incoming signal does pass  
16 these tests, then the wake up timer and logic circuit determines whether  
17 the clock recovery and data recovery circuit 38 locks on to the clock  
18 frequency contained in the chip rate of the incoming signal within a  
19 predetermined time period. If frequency lock is obtained, the  
20 microprocessor is turned on for processing of the received command.  
21 this is a processor on mode illustrated by a vertical line marked  
22 "PROCESSOR ON" in Fig. 27.

23 If frequency lock is not obtained within the predetermined time,  
24 the integrated circuit 16 returns to the sleep mode.

1 Other appropriate tests can be performed in embodiments where  
2 spread spectrum is not employed. In these embodiments, knowing how  
3 valid data is encoded, the wake up timer and logic still compares the  
4 number of transitions received in a given amount of time with an  
5 expected number of transitions for a valid signal.

6 In summary, various tests are performed, and the order in which  
7 they are performed is preferably selected to most quickly identify invalid  
8 signals. U.S. Patent Application Serial No. 08/424,827, filed April 19,  
9 1995 and U.S. Patent Application Serial No. 08/092,147, which are  
10 incorporated herein by reference, disclose tests that could be employed  
11 in various alternative embodiments of the invention.

12 After the wake up timer and logic circuit 36 determines that a  
13 received signal is valid, the integrated circuit 16 then performs clock  
14 recovery. To save space and cost, the preferred device 12 does not  
15 include a crystal timing element (clock). Instead, all timing for the  
16 device 12 is extracted from valid incoming signals received by the  
17 receiver 30.

18 In one embodiment, a valid incoming radio frequency signal is  
19 digital, and starts with a preamble, which is followed by a start code  
20 (or Barker code), which is followed by data (e.g., a command). For  
21 example, in the illustrated embodiment, the preamble is a long (e.g.,  
22 eighteen milliseconds) string of zeros; i.e., the thirty-one chip sequence  
23 is inverted, and sent repeatedly for approximately 18 milliseconds. In

24

1 the illustrated embodiment the data or command after the Barker code  
2 is shorter than the preamble, and is approximately 4 milliseconds long.

#### 3 4 Clock Recovery and Data Recovery Circuit

5 The clock for the entire integrated circuit 16 is extracted from  
6 the incoming message itself. In one embodiment, the transmitter 32 is  
7 selectable as being operable in an active transmission mode, or a  
8 backscatter mode. If the transmitter 32 is operating in an active mode,  
9 the extracted clock is multiplied up to the carrier frequency of the  
10 transmitter 32. For example, in one embodiment, the transmitter carrier  
11 frequency is 2.44 GHz. The choice of chip rate is a function of the  
12 carrier frequency and the carrier frequency has to be divisible by a  
13 power of two to give the chip rate on the input.

14 If the transmitter 32 is operating in a backscatter mode, the clock  
15 that has been recovered from the incoming signal received by the  
16 receiver 30 is divided to make it slower and is then used for frequency  
17 shift key or phase shift key modulated backscatter.

18 In summary, a clock is recovered from the incoming message, and  
19 used for timing for the micro controller 34 and all the other clock  
20 circuitry on the chip, and also for deriving the transmitter carrier or  
21 the subcarrier, depending on whether the transmitter is operating in  
22 active mode or backscatter mode.

23 Note that there are disadvantages to generating a transmit  
24 frequency in this fashion. In an alternative embodiment (not shown),

1 a crystal is employed to generate a clock. A crystal provides a more  
2 stable, reliable clock to generate the transmit frequency, but also  
3 increases cost and size of the device 12.

4 In addition to recovering a clock, the clock recovery and data  
5 recovery circuit 38 also performs data recovery on valid incoming  
6 signals. The valid spread spectrum incoming signal is passed through  
7 the spread spectrum processing circuit 40, and the spread spectrum  
8 processing circuit 40 extracts the actual ones and zeros of data from  
9 the incoming signal. More particularly, the spread spectrum processing  
10 circuit 40 takes the chips from the spread spectrum signal, and reduces  
11 each thirty-one chip section down to a bit of one or zero, which is  
12 passed to the micro controller 34.

#### 13 14 Micro controller

15 The micro controller 34 includes a serial processor, or I/O facility  
16 that received the bits from the spread spectrum processing circuit 40.  
17 The micro controller 34 performs further error correction. More  
18 particularly, a modified hamming code is employed, where each eight  
19 bits of data is accompanied by five check bits used by the micro  
20 controller 34 for error correction. The micro controller 34 further  
21 includes a memory, and after performing the data correction, the micro  
22 controller 34 stores bytes of the data bits in memory. These bytes  
23 contain a command sent by the interrogator 26. The micro  
24 controller 34 responds to the command.

1 For example, the interrogator 26 may send a command requesting  
2 that any device 12 in the field respond with the device's identification  
3 number. Status information is also returned to the interrogator 26 from  
4 the device 12 when the device 12 responds.

#### 5 6 Unalterable Identification

7 In one embodiment, the integrated circuit 16 includes unalterable  
8 indicia (a signature), different from the device's identification number  
9 discussed above. The unalterable indicia is burned into programmable  
10 read only memory or formed using a laser operating on fusible links.  
11 The unalterable indicia is indicative of the history of the particular die  
12 used to manufacture the integrated circuit 16. For example, in the  
13 illustrated embodiment, the unalterable indicia includes a lot number,  
14 wafer number, and die number of the die used to manufacture the  
15 integrated circuit 16. This information is transmitted by the transmitter  
16 in response to a manufacturer's command received by the receiver. In  
17 one embodiment, the manufacturer's command is a controlled access, or  
18 secret command that is not readily ascertainable by the public or  
19 purchaser/user of the device. This unalterable indicia can be used to



1 trace manufacturing problems in defective devices 12, or to locate stolen  
2 products carrying a device 12.

### 3 4 Arbitration

5 If the interrogator 26 sends out a command requesting that all  
6 devices 12 within range identify themselves, and gets a large number of  
7 simultaneous replies, the interrogator 26 may not be able to interpret any  
8 of these replies. Further, there may be multiple interrogators in an  
9 area trying to interrogate the same device 12.

10 Therefore, arbitration schemes are provided. With the more  
11 common scenario of multiple devices 12 trying to respond to an  
12 interrogator, the interrogator 26 sends a command causing each  
13 device 12 of a potentially large number of responding devices 12 to  
14 select a random number from a known range and use it as that  
15 device's arbitration number. By transmitting requests for identification  
16 to various subsets of the full range of arbitration numbers, and checking  
17 for an error-free response, the interrogator 26 determines the arbitration  
18 number of every responder station capable of communicating at the  
19 same time. Therefore, the interrogator 26 is able to conduct  
20 subsequent uninterrupted communication with devices 12, one at a time,  
21 by addressing only one device 12.

22 If the interrogator 26 has prior knowledge of the identification  
23 number of a device 12 which the interrogator 26 is looking for, it can  
24

1 specify that a response is requested only from the device 12 with that  
2 identification number.

3 Arbitration schemes are discussed below, in greater detail, in  
4 connection with protocols.

5 U.S. Patent No. 5,365,551 to Snodgrass et al., which is  
6 incorporated by reference, discloses arbitration schemes that could be  
7 employed in various alternative embodiments of the invention.

### 8 9 Reply

10 After the micro controller processes a command from the  
11 interrogator 26, the micro controller formats the reply as specified in  
12 the protocol and the formatted reply leaves the micro controller via a  
13 serial data port of the micro controller. If desired, the formatted reply  
14 is spread spectrum encoded by the spread spectrum processing  
15 circuit 40. The reply is then modulated by the transmitter 32. The  
16 transmitter 32 is capable of transmitting using different modulation  
17 schemes, and the modulation scheme is selectable by the interrogator 26.  
18 More particularly, if it is desired to change the modulation scheme, the  
19 interrogator 26 sends an appropriate command via radio frequency.

20 The transmitted replies have a format similar to the format of  
21 incoming messages. More particularly, a reply starts with a preamble  
22 (e.g., all zeros in active mode, or alternating double zeros and double  
23 ones in backscatter mode), followed by a Barker or start code which  
24 is thirteen bits long, followed by actual data.

1 No stop bits are included in the incoming message or reply, in  
2 the preferred embodiment. Instead, part of the incoming message  
3 describes how many bytes are included, so the integrated circuit 16  
4 knows how much information is included. Similarly, part of the  
5 outgoing reply describes how many bytes are included, so the  
6 interrogator 12 knows how much information is included. The incoming  
7 message and outgoing reply preferably also include a check sum or  
8 redundancy code so that the integrated circuit 16 or the interrogator 12  
9 can confirm receipt of the entire message or reply.

10 After the reply is sent, the integrated circuit 16 returns to the  
11 sleep mode, and the wake up timer and logic circuit 36 starts timing  
12 again for the next wake up (e.g., in 16 milliseconds, or whatever period  
13 is selected).

#### 14 15 Detailed Circuit Schematics

16 Fig. 6 is a graph illustrating how Figs. 6AA-EK are to be  
17 assembled.

18 Figs. 6AA-EK include circuitry partitioned in blocks in a manner  
19 that is somewhat different from the way the blocks are partitioned in  
20 Fig. 5. In some ways Figs. 6AA-EK shows less detail than in Fig. 5,  
21 and in some ways they show more detail.

22 The integrated circuit 16 is shown as including an analog  
23 processor "anlgproc," an RF processor "rfproc," a PN (pseudo random  
24

number) processor "pnproc," a data processor "dataproc," and return link configuration logic "rlconfig."

The data processor "dataproc" shown in Figs. 6AA-EK is the micro controller or microprocessor 34 of Fig. 5. The data processor "dataproc" is shown in greater detail in Fig. 7. In the illustrated embodiment, the data processor "dataproc" is an eight bit processor, and includes a ROM "rom," a RAM "ram," a serial I/O block "sio," an eight bit ALU (arithmetic logic unit) "alu," an instruction decoder programmable logic array "insdec," and address decoder "adrdec," a clock generator "clk," a conditional qualifier decoder "cqualdec," a databus latch/precharge circuit "dblatch," a timed lockout divider "tld," a data interleaver (which interleaves two thirteen bit words) "dil," a convolutional encoder and preamble generator "conv," a digital port output controller "doutport," a shift register input data multiplexer "shdel" and a series of registers. In the illustrated embodiment, the registers include a timed lockout register "tloreg," a plurality of status registers "sreg," a plurality of read/write control registers "oreg," and an instruction register "insreg."

The registers are used to drive control lines to various different circuits to allow the data processor to have control over those circuits. The "sio" block (described below) is the data path for data received and for the data to be transmitted.

Fig. 6.01 is a layout diagram illustrating the physical layout of various components on an integrated circuit die, in accordance with one

embodiment of the invention. The physical locations and sizes of components relative to other components are shown. Boundaries between various blocks may be approximate in the sense that portions of certain blocks may extend into other blocks. The layout diagram illustrates that separate analog and digital ground returns are provided. In the illustrated embodiment, the ground return for the receiver and transmitter is spaced apart from the receiver and transmitter. However, in an alternative embodiment, locating the ground return for the receiver and transmitter proximate the receiver and transmitter may provide improved results. In the preferred embodiment, the transmitter and receiver circuitry is physically located on the die close to an edge, proximate to the bond pads. More particularly, the microwave outputs of the transmitter 32 are arranged on the die so as to be next to (in close physical proximity to) the appropriate bond pads. Also shown in Fig. 6.01 are small squares adjacent the receiver and active transmitter pads, respectively. These are ground pads for microwave probing, in the exemplary embodiment. In an alternative embodiment, these microwave probing ground pads can be employed as functional ground pads instead of using the illustrated common analog ground pad.

Fig. 7.01AA-BB provide a circuit drawing of a processor clock generator "clk." The processor clock generator provides clock circuitry that generates all the various clocks that are used by the processor.

Figs. 7.0101AA-BB provide a circuit drawing of a processor clock controller "clkctl." The clock controller "clkctl" determines when the

1 clocks are running. As described elsewhere, the processor is not always  
2 on. The clock controller uses enabling signals from wake up so that  
3 it knows when to turn on. Thus, some of the inputs to the clock  
4 controller are power wake up, receive wake up, timer wake up. The  
5 clock controller also synchronizes shut down of the clocks when the  
6 processor has completed its task.

7 Figs. 7.0102AE-DJ provide a circuit drawing of a processor phase  
8 generator "clkph." The processor phase generator "clkph" generates  
9 master clocks - phase one "PH1" and phase two "PH2" - which are  
10 non-overlapping clocks.

11 Figs. 7.0103AA-BD provide a circuit drawing of a clock state  
12 generator "clkst." The clock state generator "clkst" generates some  
13 derivative clocks. Processor instruction cycles are divided. There are  
14 cycles and there are states. Within each cycle, which is a certain time  
15 period, there are four states - S1 through S4. The states are all non-  
16 overlapping, and each state has a high time that is one quarter of the  
17 cycle time. As a processor instruction executes, the instruction is taken  
18 from the rom "rom," and loaded into the instruction register. The  
19 instruction can be, for example, a 1, 2 or 3 cycle instruction, depending  
20 on how complex the function is that is performed by that instruction.  
21 These are micro instructions for running the processor on chip. They  
22 should not be confused with the commands that are sent by radio  
23 frequency, which are a much higher level commands. The commands  
24 sent by radio frequency require many of these micro instructions for the

processor to carry them out. During clock cycle one, line C1 in Figs. 7.0103AA-BD is high, during clock cycle two, line C2 is high, etc. Within each one of those clock cycles, state one is high for a certain time period and then goes low, and state two goes high for a certain time period then goes low, and so on up through state four. Within each of these states, there is one phase one high time, and one phase two high time.

Figs. 7.02AA-BF provide a circuit drawing of an address decoder "adrdec." In executing instructions, the processor has the need to move bytes of data between registers and ram "ram" and possibly to the serial IO controller "sio." The address decoder "adrdec" generates enable lines to those various different blocks (the registers, ram, and sio, as appropriate) when their address appears on the address bus. The primary input to the address decoder is the address bus. This decoder decides which circuit block is being addressed and issues an enable for either a write or a read, whichever is appropriate, to that particular block.

Figs. 7.03AA-EH provide a circuit drawing of random access memory "ram." The ram has 512 bytes of storage available. 256 of those bytes are available to the user of the device 12, and the other 256 bites are used to do calculations required by the processor. Most of the drawing is taken up by blocks of RAM arrays "ram8x4."

Figs. 7.0301AA-BB provide a circuit drawing of a ram control circuit "ramctl." The ram control circuit issues word line select enable

1 signals, a read command, a write command, and some precharge signals.  
2 The ram control circuit generates the signals to control access to and  
3 from the random access memory "ram."

4 Figs. 7.0302AA-AC provide a circuit drawing of a RAM array  
5 "ram 8x4." Each RAM array is made up of four rows and eight  
6 columns of RAM cells.

7 Fig. 7.030201 provides a circuit drawing of a single RAM cell.  
8 In the illustrated embodiment, the RAM cell is a six transistor RAM  
9 cell. Four transistor RAM cells are employed in alternative  
10 embodiments.

11 Figs. 7.0303AA-AD provide a circuit drawing of a RAM precharge  
12 circuit "rampch." Figs. 7.0304AA-AD provide a circuit drawing of a  
13 RAM precharge circuit "ramdch." In the illustrated embodiment, this  
14 circuit has been disabled as is shown in the figure. The RAM  
15 precharge circuits provides precharge signals to speed up writing to and  
16 reading from RAM cells.

17 Fig. 7.0305 provides a circuit drawing of a RAM address buffer  
18 "ramadb." The RAM address buffer isolates the capacitive load  
19 presented by the RAM circuits from the address bus.

20 Figs. 7.0306AA-BA provide a circuit drawing of a RAM word line  
21 driver "ramwdr." The RAM wordline driver is a predecoder. It takes  
22 two address inputs and generates four possible select lines "P0-P3"  
23 which are used in a row decoder (discussed below) for the RAM.  
24



1 Figs. 7.0307AA-BB provide a circuit drawing of a RAM word line  
2 decoder "ramwdec." The RAM word line decoder receives the select  
3 lines from the RAM wordline driver in conjunction with four other  
4 addresses "AD0-AD3" to select a unique word line. A word line is a  
5 row of RAM cells within the RAM.

6 Figs. 7.0308AA-BB provide a circuit drawing of a RAM column  
7 select decode circuit "ramcdec." The RAM column select decode circuit  
8 uses three address lines "AD5-AD7" to generate eight select lines  
9 "CSEL0-CSEL7."

10 Figs. 7.0309AA-BG provide a circuit drawing of a RAM column  
11 selector multiplexor "ramcsel." The RAM column selector multiplexor  
12 uses the output select lines "CSEL0-CSEL7" from the RAM column  
13 select decode circuit "ramcdec" to connect one pair of bit or column  
14 lines out of eight pairs "BIT0N/P"-"BIT7N/P" onto a bus. The bus  
15 goes to a sense amp or to a write driver, depending on whether a  
16 RAM cell is being read or written. There are eight of these RAM  
17 column selectors side by side, functioning in the same manner. With  
18 any one selection, one of eight pairs are selected on Figs.  
19 7.0309AA-BG, but there are seven more similar selections taking place  
20 so an entire byte of RAM is selected at one time.

21 Figs. 7.0310AA-BB provide a circuit drawing of a RAM databus  
22 interface "ramdb." The RAM databus interface includes a sense amp  
23 and write driver for the RAM. The RAM databus interface receives  
24



address inputs "A7-A9" and generates enable signals "WDR0-WDR7" to select row lines of the ROM.

Figs. 7.0404AA-DC provide a circuit drawing of a ROM word block decoder "romwdec\_rev." The ROM word block decoder has as inputs the enable signals "WDR0-WDR7" from the ROM word line driver "romwdr" plus other addresses to generate actual word line signals themselves. A word line signal selects a row of ROM cells.

Figs. 7.0405AA-BA provide a circuit drawing of a ROM bit line address driver "romblldr." The ROM bit line address driver buffers some of the addresses so they are capable of driving a large decoder structure "rombldec" (described below).

Figs. 7.0406AA-CK provide a circuit drawing of a ROM bit line decoder "rombldec." The ROM bit line decoder provides a decoder structure for selecting a particular ROM bit line out of thirty-two bit lines. There are eight such "rombldec" circuits, allowing simultaneous selection of eight bit lines.

Figs. 7.0407AA-AB provide a circuit drawing of a ROM sense amplifier "romsns." The ROM sense amplifier is the sense amp used for determining the state of a particular ROM bit being accessed. Eight ROM bit sense amplifiers are used.

Figs. 7.05AA-CB provide a circuit drawing of an instruction register "insreg." The code or program that controls the operation of the processor is stored in the ROM. The instructions stored in the ROM are transferred one at a time to this instruction register "insreg"

1 so that they can be interpreted and the processor can carry out the  
2 operations required by that instruction. After the integrated circuit  
3 wakes up, its operation is controlled by the wake up and clock recovery  
4 circuits. After the integrated circuit locks on to the clock and a valid  
5 start (Barker) code is received, the processor turns on and the program  
6 stored in the ROM takes over from that point. The program performs  
7 functions such as determining if the integrated circuit 16 is in a power  
8 up cycle. If the device 12 is in a power up cycle, the processor  
9 performs various tasks relevant to power up. If the integrated circuit  
10 16 is receiving a command from an interrogator, the program will  
11 determine which command and then go through a sequence of required  
12 steps in order to respond appropriately to that command. Then the  
13 program allows the integrated circuit 16 to go back to sleep.

14 Figs. 7.0501AA-BB provide a circuit drawing of an instruction  
15 register "insrcel" included in the instruction register "insreg."

16 Figs. 7.06AA-CN provide a circuit drawing of an instruction  
17 decoder PLA "insdec." The instruction decoder PLA interprets what is  
18 in the instruction register "insreg" and issues all the enable signals  
19 necessary to effect performance of the functions called for in that  
20 instruction. Details of the instruction decoder PLA are shown in Figs.  
21 7.0601AA-HI; 7.0602AA-JH; 7.0603AA-JI; and 7.0604AA-JI.

22 Figs. 7.0601AA-HI provide a circuit drawing of an instruction  
23 decoder (first section) "insdec1."

Figs. 7.0602AA-JH provide a circuit drawing of an instruction decoder (second section) "insdec2."

Figs. 7.0603AA-JI provide a circuit drawing of an instruction decoder (third section) "insdec3."

Figs. 7.0604AA-JI provide a circuit drawing of an instruction decoder (fourth section) "insdec4." Fig. 7.060401 provides a circuit drawing of an instruction decoder ROM amp "insramp" included in the circuit of Figs. 7.0604AA-JI, 7.0601AA-HI, 7.0602AA-JH, and 7.0603AA-JI. Fig. 7.060402 is a circuit drawing of an instruction decoder PLA amp "inspamp" included in the circuit of Figs. 7.0604AA-JI, 7.0601AA-HI, 7.0602AA-JH, and 7.0603AA-JI. Fig. 7.060403 is a circuit drawing of an instruction decoder PLA latch "insplat" included in the circuit of Figs. 7.0604AA-JI, 7.0601AA-HI, 7.0602AA-JH, and 7.0603AA-JI.

Figs. 7.07AA-BB provide a circuit drawing of a conditional qualifier decoder "cqualdec." Certain instructions behave differently depending on certain conditions (e.g., whether a carry bit is set), and the conditional qualifier decoder looks for these conditions.

Figs. 7.08AA-CA provide a circuit drawing of a databus latch and precharge circuit "dblatch." Data is bused around in eight bit bytes, and the databus latch and precharge circuit drives the databus. The data bus is in a precharge high state when the data bus is not being used. Whichever source of data is selected to put its information on the bus will then drive selected bits low if appropriate.

1 Figs. 7.09AA-BF provide a circuit drawing of an arithmetic logic  
2 unit "alu." The arithmetic logic unit "alu" is a basic arithmetic logic  
3 unit that provides enough flexibility to perform the functions that are  
4 needed for the RFID task. Details of the arithmetic logic unit are  
5 provided in drawings below.

6 Figs. 7.0901AA-CE provide a circuit drawing of an ALU low byte  
7 "alubyt1". There are eight bits within the ALU low byte that are all  
8 processed simultaneously.

9 Figs. 7.090101AA-AD provide a circuit drawing of a ALU bit  
10 "alubit1" included in the ALU low byte "alubyt1." Figs. 7.090101AA-AD  
11 show the registers contained within each bit of the ALU. The registers  
12 include an A cell "aluacell" and a B cell "alubcell" which are the  
13 primary registers. The data on which arithmetic or logical operations  
14 are to be performed reside typically in the A cell "aluacell" or the B  
15 cell "alubcell." The registers further include a program counter "alupc,"  
16 a stack pointer "alurcell," a data pointer "alurcell," and a memory  
17 address register "alumar" that provides for indirect addressing. The  
18 ALU bit "alubit1" further includes an adder "aluadd" and a slave  
19 register "aluslave" to the adder.

20 Fig. 7.09010101 is a circuit drawing showing details of construction  
21 of an ALU bit decoder cell "alubdec" included in the ALU bit.

22 Fig. 7.09010102 is a circuit drawing showing details of construction  
23 of the ALU B register cell "alubcell" included in the ALU bit.  
24

1 Fig. 7.09010103 is a circuit drawing showing details of construction  
2 of the ALU A register cell "alubacell" included in the ALU bit.

3 Fig. 7.09010104 is a circuit drawing showing details of construction  
4 of the ALU program counter "alu pc" included in the ALU bit.

5 Fig. 7.09010105 is a circuit drawing showing details of construction  
6 of the ALU register cell "alurcell." Such cells are used for a stack  
7 pointer, data pointer, etc.

8 Fig. 7.09010106 is a circuit drawing showing details of construction  
9 of the ALU memory address register "alumar" included in the ALU bit.

10 Fig. 7.09010107 is a circuit drawing showing details of construction  
11 of the ALU slave cell "aluslave" for the ALU adder "aluadd."

12 Fig. 7.09010108 is a circuit drawing showing details of construction  
13 of the ALU adder "aluadd" included in the ALU bit.

14 Figs. 7.0902AA-BD provide a circuit drawing for an ALU high  
15 byte "alubyth" which functions similarly to the ALU low byte "alubyt1."  
16 Two ALU bytes are provided so that sixteen bit commands can be  
17 processed.

18 Figs. 7.090201AA-AC provide a circuit drawing of a bit "alubith"  
19 included in the ALU high byte "alubyth."

20  
21 Details of Low Power Dormant Mode

22 It is sometimes desirable to prevent the integrated circuit 16 from  
23 responding to commands from an interrogator. For example, after  
24 communication with a particular device 12, it is sometimes desirable to

1 prevent that particular device 12 from responding to a subsequent  
2 interrogation that is intended for a different device 12. If, for example,  
3 the device 12 is used in connection with an access gate, after an  
4 interrogator has read a badge containing the device 12 as a controlled  
5 access point is passed, the interrogator no longer has a need to  
6 communicate with that badge. The interrogator instead would want to  
7 pick up subsequent badges passing through the access gate. In addition,  
8 when the interrogator no longer has a need to communicate with a  
9 particular device 12, it is desirable that the device 12 stay in the sleep  
10 mode to conserve battery power.

11 In one embodiment, the device 12 is put into an unresponsive  
12 state by using a counter which is set to a desired time via a radio  
13 frequency command. The device will then not respond to Identify  
14 commands (described below in greater detail) used by an interrogator  
15 to request information from a device 12. In this embodiment, the  
16 unresponsive state can be cancelled by a radio frequency command.  
17 However, this embodiment is disadvantageous in that the device must  
18 wake up to process incoming commands and abort if the command is  
19 an Identify command. This consumes battery capacity.

20 In a preferred embodiment, the device 12 can be placed in a  
21 dormant mode via a radio frequency command. The dormant mode  
22 cannot be cancelled. When in the dormant mode, the device 12 does  
23 not wake up to look for incoming commands.  
24



1 Figs. 7.10AA-CC provide a circuit drawing of a timed lock out  
2 divider "tld." The timed lock out divider takes as an input the low  
3 power clock which is the same clock that sets the wake up interval for  
4 the integrated circuit 16. The timed lock out divider provides two  
5 functions. The timed lockout divider provides an alarm timer function,  
6 and provides a timed lockout function which is used for the dormant  
7 mode function and for the timed lockout of Identify commands.

8 The alarm timer is set to go off in intervals, such as about every  
9 one minute. As an alarm timer, the timed lock out divider causes the  
10 integrated circuit 16 to wake up and check for threshold violations in  
11 alarm mode. Such threshold violations would be triggered by analog  
12 sensors such as temperature sensors, magnetic sensors, etc.

13 The timed lock out divider also allows, by RF command from an  
14 interrogator, a user to disable a device 12 to make it not respond for  
15 a prescribed period of time (i.e., allows the user to place the device  
16 12 in the dormant mode). The prescribed period of time can be set  
17 in various increments. For example, in the illustrated embodiment, the  
18 increments are one second increments from one up to 255 seconds.

19 When in the dormant mode, the device 12 does not periodically  
20 switch to the receiver on mode to check for the presence of radio  
21 frequency commands. Therefore, power is conserved.

22 This dormant mode function is useful for the same reasons that  
23 the cancellable timed disabling is useful. If, for example, the device  
24 12 is used in connection with an access gate, after an interrogator has

1 read a badge containing the device 12 as a controlled access point is  
2 passed, the interrogator no longer has a need to communicate with that  
3 badge. The interrogator instead would want to pick up subsequent  
4 badges. Therefore, the interrogator can instruct the device 12 to not  
5 respond for a certain time, so as to prevent an unwanted response of  
6 a device 12, after having communicated with that device 12, but with  
7 increased power savings over the cancellable timed disabling. Because  
8 wake ups are disabled, current consumed by the device 12 is very low;  
9 e.g., 1  $\mu$ A.

10 Fig. 7.1001 provides a circuit drawing showing details of  
11 construction of a timed lock out divider cell "tldcel" included in the  
12 timed lockout divider "tld."

13 Figs. 7.11AA-AB provide a circuit drawing of a timed lock out  
14 register "tlorege." This register acts as a down counter and is selectively  
15 set with the desired lockout time, from 1 to 255 seconds.

16 Figs. 7.1101AA-AC provide a circuit drawing of a timed lock out  
17 register cell "tlorcel" included in the timed lockout register.

18 Figs. 7.12AA-AC provide a circuit drawing of an read/write control  
19 register or output register "oreg." There are a number of these output  
20 registers. The output registers allow the processor to send control  
21 signals out to various peripheral circuits to cause them to function when  
22 required.

23 Fig. 7.1201 provides construction details of a control register cell  
24 "regcell" included in the output register "oreg."

1 Figs. 7.13AA-BA provide a circuit drawing of a status register  
2 "sreg." The processor uses the status register to monitor the status of  
3 lines supplied from various blocks of circuitry.

4 Figs. 7.1301AA-AB provide a circuit drawing of a status register  
5 cell "sregcel" included in the status register.

6 Figs. 7.14AA-AB provide a circuit drawing of a serial input output  
7 block "sio." The serial input output circuitry is the data path for data  
8 received and for the data to be transmitted. This circuit controls the  
9 transfer of the serial stream of data received from the receiver into the  
10 processor. The circuit also controls the transfer of the transmit serial  
11 data stream from the processor out to the transmitter. The serial input  
12 output circuitry comprises two blocks: a block "siodata" that processes  
13 data, and a controller "siocctl" that runs the block that processes data.

14 Figs. 7.1401AA-AB provide a circuit drawing of a serial input  
15 output data path "siodata." When the integrated circuit 16 is in a  
16 transmit mode, data enters the bit registers "sioreg" from the top of  
17 the figure, and the data is transferred down to the registers "siobdlat"  
18 and "siobdlat\_inv" which are the row of blocks second up from the  
19 bottom of the figure. The intermediate stages "sioxor" are all exclusive  
20 or gates that are used to generate check bits according to the  
21 previously mentioned modified Hamming code. The extra five bits "P0-  
22 P4" appended to the eight data bits "D0-D7" are generated by the  
23 exclusive-or gates, and then all thirteen bits are transferred to the  
24 registers "sioshr" which are the row of blocks at the bottom of the

figure. The thirteen bits are serially shifted out to the right of the figure.

When the integrated circuit 16 is in a receive mode, a reverse sequence takes place. Data is shifted into the thirteen bit registers "sioshr" shown on the bottom of the figure, then transferred up to the registers "siodblat" immediately above the shift registers "sioshr" in the figure. Then the exclusive or circuitry "sioxor" uses the data and the check bits to determine whether there are any errors. If there are any correctable errors, they are corrected at that point. The serial input output data path "siodata" can also detect double bit errors which are not correctable. If a double bit error is detected, a signal is provided at the upper left of the figure to the processor that an uncorrectable error has occurred. Assuming that there is no uncorrectable error, the eight corrected bits are now present as inputs to the top row of registers "sioreg." The eight corrected bits are then transferred in to the top row of registers. From the top row of registers "sioreg," the corrected bits are transferred in parallel to the processor.

Figs. 7.140101AA-AB provide construction details of the serial input output register cell "sioreg" included in the serial input output data path "siodata."

Figs. 7.140102AA-GF provide construction details of the serial input output exclusive or circuit "sioxor" included in the serial input output data path "siodata."

Figs. 7.140103AA-AB provide construction details of the bidirectional latch "siobdlat\_inv" included in the serial input output data path "siodata."

Figs. 7.140104AA-BB provide construction details of the shift register "sioshr" included in the serial input output data path "siodata."

Figs. 7.140105AA-AB provide construction details of the bidirectional latch "siobdlat" included in the serial input output data path "siodata."

Figs. 7.1402BA-EI provide a circuit drawing of the previously mentioned control logic "sioctl." The control logic "sioctl" generates all the clocking and the signals that control when data is transferred from register to register.

Figs. 7.140201AA-BB provide a circuit drawing showing construction details of the counter bit "siocbit" included in the control logic "sioctl."

Figs. 7.15AA-EC provide a circuit drawing of a data interleaver "dil." In a number of modulation schemes used or selectively used by the integrated circuit 16, differential encoding is employed. Use of differential encoding in the integrated circuit 16 makes possible a simpler receiver in the interrogator. However, if an error occurs in the process of differential encoding, it necessarily corrupts two adjacent bits. The modified Hamming code cannot correct errors where two adjacent bits are in error. This problem is solved by interleaving two bytes. Bit by bit, the first bit of one byte is shuffled next to the first bit of another byte and so on through all thirteen bits. This way, when

1 differential encoding is performed, which may possibly create two  
2 adjacent errors, the two bytes are deinterleaved and separated at the  
3 receiver so that the bytes are in separate error corrective words. The  
4 errors can then be fixed.

5 The data interleaver works by shifting data in from a data input  
6 "SIOTXD" (on the upper left of Figs. 7.15AA-EC). Twenty-six bits are  
7 shifted into the registers "dil\_sreg" shown along the top of Figs.  
8 7.15AA-EC, then all twenty-six bits are simultaneously shifted to the  
9 lower registers "dil\_plsreg" and scrambled in order simultaneously by  
10 wiring interconnections between the registers "dil\_sreg" and the registers  
11 "dil\_plsreg" shown in Figs. 7.15AA-CC. Thus, a new interleave order  
12 is generated on transfer from the registers "dil\_sreg" to the registers  
13 "dil\_plsreg." Then, the contents of the registers "dil\_plsreg" are shifted  
14 out (to the right in the view of Figs. 7.15AA-EC) in a serial, bit by  
15 bit fashion, through line "DILTXD."

16 Figs. 7.1501AA-CA provide a circuit drawing showing construction  
17 details of the shift register "dil\_sreg" included in the data interleaver  
18 "dil."

19 Figs. 7.1502AA-CA provide a circuit drawing showing construction  
20 details of the parallel load shift register "dil\_plsreg" included in the  
21 data interleaver "dil."

22 Fig. 7.150201 provides a circuit drawing showing construction  
23 details of a shift register bit "dil\_sregbit" included in the parallel load  
24 shift register "dil\_sregbit" and in the shift register "dil\_sreg."

1 Figs. 7.16AA-CD provide a circuit drawing of a convolutional  
2 encoder "conv." In the illustrated embodiment, convolutional encoding  
3 is disabled. However, in one embodiment, convolution encoding is  
4 provided. The circuitry of Figs. 7.16AA-CD performs more functions  
5 than just convolutional encoding. The circuitry of Figs. 7.16AA-CD also  
6 includes a preamble generator. In one embodiment, a series of zeros  
7 are generated as a preamble. However, in the illustrated embodiment,  
8 a pattern of alternating zeros and ones (0101) is generated for DPSK  
9 backscatter. The circuitry of Figs. 7.16AA-CD also includes a clock for  
10 the SIO "sio."

11 Fig. 7.1601 provides a circuit drawing showing construction details  
12 of a shift register cell "convshr" included in the convolutional encoder  
13 "conv."

14 Fig. 7.1602 provides a circuit drawing showing construction details  
15 of a summer "convsum" included in the convolutional encoder "conv."

16 Figs. 7.17AA-BB provide a circuit drawing of a shift register data  
17 multiplexor "shdcel." The shift register data multiplexor provides a port  
18 into the processor. It does a selection among eight sources on the  
19 integrated circuit 16, and connects only one of them for shifting of data  
20 for transfer into the A register.

21 Figs. 7.18AA-CC provide a circuit drawing of a digital port output  
22 controller "doutport." The device selectively reads data via a digital  
23 port in response to a radio frequency command, instead of by radio  
24 frequency reception, and the device selectively writes data via a digital

1 port in response to a radio frequency command, instead of by radio  
2 frequency. The digital port output controller circuit controls these  
3 functions. The digital port output controller circuit also includes a  
4 clock in order to synchronize the transfer of the data in either direction  
5 (input or output).

6 The RF processor "rfproc" shown in Figs. 6AA-EK contains the  
7 receiver 30, the transmitter 32, the clock recovery and data recovery  
8 circuit 38, and the wake up timer and logic circuit 36. The RF  
9 processor "rfproc" is shown in greater detail in Figs. 8AA-CB.

10 Figs. 8AA-CB provide a circuit drawing of a RF processor  
11 "rfproc." The RF processor "rfproc" includes a receiver "rx" (which is  
12 the receiver 30 of Figs. 6AA-EK), a transmitter "tx" (which is the  
13 transmitter 32 of Figs. 6AA-EK), a low power frequency locked loop  
14 "lpfl," a counter bit "lpfl\_cbit," a receiver wake up controller "rxwu"  
15 (which is the wake up timer and logic circuit 36 of Figs. 6AA-EK), and  
16 a digital clock and data recovery circuit "dcr" (which is the clock and  
17 data recovery circuit 38 of Figs. 6AA-EK). Thus, RF processor "rfproc"  
18 includes the clock that sets the wake up interval, as well as logic that  
19 performs tests on the incoming signal to see whether the incoming  
20 signal is a valid signal such that the integrated circuit 16 should stay  
21 awake.

22 Figs. 8.01AA-DE provide a circuit drawing of the receiver "rx"  
23 included in the RF processor. In the illustrated embodiment, the  
24 receiver "rx" includes a Schottky diode detector "diodedet." In the



illustrated embodiment, the Schottky diode detector "diodet" is an inductorless Schottky diode detector. Instead of employing inductors in the diode detector to supply bias current to the diode, the diode detector includes a current source which drives current through both an antenna and a Schottky diode included in the detector. The inductorless Schottky diode detector is described in more detail below. Figs. 8.01AA-DE also illustrate a CMOS detector "cmosdet" that is used in accordance with an alternative embodiment, but which is not used in the illustrated embodiment. The output of the Schottky diode detector is applied through a series of AC coupled amplifiers. More particularly, in the illustrated embodiment, the Schottky diode detector is applied through amplifiers "videoamp1," "videoamp2" replicated four times, and then into a comparator. The function of the comparator is to put out a full digital signal. The output of the comparator is a base band digital representation of the command that was sent by the interrogator.

A base band signal is a signal without a carrier frequency present. The output of the comparator is a signal that is the equivalent of the signal that was used to modulate the carrier back at the interrogator.

The receiver "rx" includes a RF detect circuit "rxdetect." The RF detect circuit determines when a modulated radio frequency signal is present at the receiver and the output of the receiver is switching between high and low states. The receiver "rx" includes a bias block "rxbias" that provides currents to the various amplifiers "videoamp1," "videoamp2," etc. The receiver "rx" further includes logic that bypasses

1 the receiver when a user selects not to use RF for an input, but rather  
2 to provide a base band input signal directly in digital form. The user  
3 may make the selection to bypass the receiver, for example, for testing  
4 or exercising the integrated circuit 16. The user may also make the  
5 selection in applications where the receiver portion of the chip is not  
6 required, but the integrated circuit 16 is used to transmit information  
7 (e.g., for periodic transmissions).

## 8 9 Schottky Diode RFID Detector

### 10 Overview

11 For purposes of realizing a cost effective and low power radio  
12 frequency receiver on an RFID tag, a simple Schottky diode receiver  
13 is utilized. The receiver is formed from a Schottky diode detector, an  
14 amplifier, and the receiving antenna "rxantenna". With the  
15 implementation of a single integrated circuit 16 RFID tag, an easy and  
16 low cost technique for configuring the frequency of operation on a tag  
17 is needed. Receiver frequency characteristics can be tailored by  
18 selecting an appropriately sized antenna to be coupled to the integrated  
19 circuit 16 that supports the Schottky diode detector. Furthermore,  
20 adjustment of bias current across the Schottky diode can be used to  
21 realize a desired resistance there across, enabling tuning or detuning of  
22 the receiver.

1 For purposes of enabling simplified representation, Fig. 29  
2 illustrates a simplified circuit schematic for one embodiment of a  
3 receiver 80 having a Schottky diode detector 84 and antenna 44.

4 The detector 84 includes a Schottky diode 86 having an anode  
5 connected to the antenna 44 and having a cathode.

6 The exemplary antenna 44 is formed from a loop or folded dipole  
7 construction. The antenna 44 performs band pass filtering.

8 The detector 84 further includes an ideal current source 88  
9 connected to the cathode of the Schottky diode 86 and driving current  
10 through the antenna and Schottky diode 86 in the direction from the  
11 anode to the cathode. The current source 88 is an ideal current source,  
12 and is configured to forward bias the Schottky diode 86, realizing a  
13 desired resistance (or impedance) in the process.

14 The detector 84 further includes a capacitor 90 connected between  
15 the cathode of the Schottky diode 86 and ground. The capacitor 90  
16 provides a radio frequency short to ground so that all radio frequency  
17 voltage appears across the Schottky diode 86. This maximizes a base  
18 band signal produced by the Schottky diode 86.

19 The detector 84 further includes a capacitor 92 having a first  
20 terminal connected to the cathode and having a second terminal defining  
21 an output of the detector 84. The capacitor 92 provides an AC short  
22 to video frequency, and defines the output of the detector 84. The  
23 capacitor 92 allows different bias levels in the detector and at the input  
24 of a video amplifier connected to the output of the detector 84.



of Fig. 3), after which the integrated circuit 16 is bonded to the antenna, as well as to the battery, using a conductive epoxy.

Preferably, the antennas 44 and 46 are printed onto the back side of the card or stamp, forming each microstrip loop antenna thereon. For example, the antenna can be silk screened onto the card with a conductive polymer thick film. Alternatively, a conductive silver filled epoxy can be used. Alternatively, the antenna can be formed from a separate piece of conductive material, for example, from a piece of wire or conductive ribbon that is glued to the back of the card.

One exemplary technique for assembling the postage stamp 20 of Fig. 4 is provided here below. The same technique can be used to assemble the badge 10 of Fig. 2, or any other similarly constructed tag having a rigid support or substrate similar to plastic cards 11 and 21. First, antennas 44 and 46 (of Fig. 5) are mounted to a back face of the card. Preferably, the above elements are simultaneously printed onto the back of a large sheet of plastic with a conductive silver printed thick film, after which the cards are individually separated, or cut from the sheet. Pads on the integrated circuit 16 form enlarged connection points for electrically bonding each antenna 44 and 46 to "rxantenna - Pad D" and "txantenna - Pad AA" of Fig. 6 and for connections to a power supply. Next, the card is positioned front face down onto a rigid support plate. Then integrated circuit 16 (of Fig. 4) is mounted to the pads with conductive beads of epoxy. Finally, the battery 18 is bonded along its bottom face with a bead of conductive

1 epoxy, after which conductive epoxy is used to electrically connect the  
2 opposite terminal or top of the battery with a corresponding conductive  
3 die pad.

4 Subsequently, a metal dam sized to conform generally to the outer  
5 peripheral shape of the card 20 is placed over the back of the card.  
6 The dam functions as an outer template while a thin layer of non-  
7 conductive epoxy (not shown) is applied to the back of the card 20,  
8 preferably hermetically sealing in the integrated circuit 16, antenna and  
9 battery. Preferably, the thin coat of epoxy consists of a coating, barely  
10 thick enough to cover over the components forming the device. One  
11 benefit provided by this construction technique is the elimination of any  
12 visible bumps in the tag which can result when constructing the tag by  
13 heat sealing two or more pieces of plastic card together to trap the  
14 device 12 therein. However, a lesser preferred construction of this  
15 invention envisions forming the tag, e.g. badge 10, stamp 20, or some  
16 other tag, with such a heat sealed sandwich of plastic cards.

17 <sup>Sub</sup> ~~By~~ Preferably, the above technique for mounting integrated circuit 16  
18 to card 20 (of Fig. 4) consists of a flip-chip mounting technique. One  
19 example of a flip-chip mounting technique is disclosed in pending U.S.  
20 Patent Application Serial No. 08/166,747, "Process of Manufacturing an  
21 Electrical Bonding Interconnect Having a Metal Bond Pad Portion and  
22 Having a Conductive Epoxy Portion Comprising an Oxide Reducing  
23 Agent," listing Rick Lake and Mark E. Tuttle as inventors, and  
24 incorporated herein by reference.

## Integrated Circuit Implementation

According to Fig. 8, the Schottky diode detector "diodet" is configured within receiver "rx" to receive radio frequency signals via receiving antenna "rxantenna". One exemplary receiving antenna configuration is depicted in Figure 5, denoted generally by reference numeral 44. In operation, the Schottky diode detector and the receiving antenna cooperate to form a tunable receiving circuit. Signals detected by the Schottky diode detector are input to a five stage amplifier, then a comparator, for further signal conditioning. The output of the comparator is a digital representation of the received baseband signal.

As shown in Fig. 8, receiver "rx" is an Amplitude Shift Keying (ASK) receiver. This is also known as an AM receiver. The illustrated embodiment employs On Off keying (OOK) wherein a digital one ("1") is represented by the presence of the RF carrier, and wherein a digital zero ("0") is represented by the absence of the carrier.

Figs. 8.01AA-DE illustrate in greater detail the circuit implementation of receiver "rx". According to this embodiment, Schottky diode detector "diodedet" receives input signals via an input "rxantenna," and bias voltages for the current source via a pair of inputs "bias1" and "bias2". A pair of output signals "OUTN" and "OUTP" leave "diodedet" for input to a serially connected chain of amplifiers, and a comparator. The array of amplifiers comprise five video amplifiers, labeled "videoamp1" and "videoamp2". Bias voltages are applied to

"bias1" and "bias2" via "rxbias," a bias circuit which generates all bias voltages required by the receiver.

A circuit "rxdet" shown in Figs. 8.01AA-DE receives the output signal from the comparator, via combinational logic, with "digrxdata" and "digrx". The output signal "RFDET" is driven high if there is a signal at the output of the comparator. The resulting signal input into "rxdet" is received via "dataIn." Additional inputs to "rxdet" include "lowrate," "Vref," "Vbias1," "Vbias2," "Vreg," and "enable." Further details of "rxdet" are disclosed below with reference to Figs. 8.0106AA-CD, entitled "RF Detect".

Figs. 8.0101AA-CB illustrate one embodiment for realizing the Schottky diode detector "diodedet" of Figs. 8.01AA-DE. Namely, a Schottky diode is forward biased from receiving antenna, coupled at "ANT," to a detector output "OUTP." A second Schottky diode is forward biased from Vdd to a detector output "OUTN." Two current sources are formed by four transistors, and are driven by bias voltages at "bias1" and "bias2." A capacitor is coupled to Vss, between each Schottky diode and associated output, "OUTP" and "OUTN," respectively. Furthermore, an array of parallel capacitors are provided in series between each Schottky diode and associated output, "OUTP" and "OUTN," respectively. The array of parallel capacitors acts as a single capacitor. Each Schottky diode is formed from an array of Schottky diodes. In order to use standard contact hole sizes, each Schottky



1 diode is formed from an array of Schottky diodes connected together  
2 in parallel to act as a single Schottky diode.

3 According to Figs. 8.01AA-DE, "OUTP" and "OUTN" are input  
4 into a multiple (e.g., five) stage amplifier and into a comparator. In  
5 order to avoid amplification of substrate noise, a differential amplifier  
6 is employed for each stage of the multiple stage amplifier. Noise  
7 appears equally on both inputs of each differential amplifier, and, the  
8 common mode rejection of the differential amplifiers impedes  
9 transmission of substrate noise. The differential amplifiers amplify a  
10 received baseband signal up to a digital level. A dummy Schottky  
11 diode (the lower Schottky diode in the figures) is connected to the  
12 second input of the first differential amplifier.

#### 13 14 Details of Realization of Wide Carrier Frequency Bandwidth

15 In order to meet the wide range of intended applications, it is  
16 desirable to construct the integrated circuit for an RFID tag to realize  
17 operation of a wide range of carrier frequencies. For example, several  
18 desirable carrier frequencies for the device disclosed in Figs. 5 and 6  
19 are 915, 2450, and 5800 MegaHertz bands. Frequency selectivity is  
20 realized in the device of Figs. 5 and 6 by appropriately configuring  
21 external antennas and internal circuit components of the integrated  
22 circuit. For the case of a single integrated circuit with an active on-  
23 board transmitter, it is necessary to design circuit components into the  
24 integrated circuitry prior to mounting and encapsulation of the integrated

1 circuit with an antenna inside of a package. Hence, the circuit  
2 components needed to facilitate tailoring of the carrier frequency must  
3 be "designed in" the integrated circuit. In the case of a backscatter  
4 transmitter, components included in the integrated circuit can be selected  
5 so as to allow operation over a wide range of carrier frequencies, the  
6 selection being made by choice of antenna.

7 According to Figs. 8.01AA-DE, the number of amplifiers that need  
8 to be implemented via "videoamp1" and "videoamp2" is determined based  
9 upon the magnitude of the minimum detected signal and the required  
10 signal to noise (S/N) ratio. Amplification is sufficient to produce full  
11 digital levels at the output of the comparator.

12 The capacitor configured to ground in the video receiver circuit  
13 of Fig. 29 (and Figs. 8.0101AA-CB) is used to separate the radio  
14 frequency (RF) from the "VIDEO AMP" side of the video receiver  
15 circuit. The capacitor is sized to impart an effective short circuit to  
16 ground at radio frequency, thereby ensuring that all of the radio  
17 frequency (RF) voltage appears across the Schottky diode terminals.  
18 Additionally, the capacitor should be sized small enough at video  
19 frequencies, so that the capacitor does not load down the video amp  
20 circuit.

21 The capacitor configured in series in the video receiver circuit of  
22 Fig. 29 (and Figs. 8.0101AA-CB) is used to block out the DC  
23 component of a voltage to "VIDEO AMP" while retaining the AC  
24

1 component. In this manner, the series capacitor forms a "blocking"  
2 capacitor or "coupling" capacitor.

#### 3 4 Details of Inductorless RF Detector

5 A second desirable feature for the integrated circuit of an RFID  
6 tag is to eliminate the need to use inductors when constructing the  
7 Schottky diode detector. One technique for providing a bias current to  
8 a Schottky diode is disclosed in Fig. 28. Fig. 28 illustrates a  
9 receiver 60 including an antenna 62 and a Schottky diode detector 64.  
10 The receiver 60 includes inductors 68 and 70 used to provide the bias  
11 current via voltage source 74 with this implementation. A capacitor 76  
12 is shunted to ground, and a second capacitor 78 is placed in series,  
13 providing AC coupling to the video amplifier. Several variations of  
14 such inductor-based bias current implementations are described in a  
15 paper entitled "Designing Detectors for RF/ID Tags," by Raymond W.  
16 Waugh of Hewlett-Packard Company, submitted for presentation at the  
17 RF Expo, San Diego, February 1, 1995, and which is already  
18 incorporated by reference. Inductors are required in all of these  
19 constructions, but their implementation on an integrated circuit proves  
20 difficult because of problems inherent in forming inductors in an  
21 integrated circuit. The circuit in Fig. 29 eliminates the inductors by  
22 biasing the Schottky diode with a high impedance current source. A  
23 current sink is provided by connecting the far end of the antenna to  
24 Vdd.

1 Details of Elimination of Overdrive Problem

2 The Schottky diode detector circuit implementation of Figs.  
3 8.0101AA-CB realizes a technique for negating the effect of high power  
4 radio frequency (RF) input levels on the Schottky diode detector. More  
5 particularly, when high level radio frequency (RF) power is present at  
6 the antenna "rxantenna," e.g. when the RFID tag antenna is close to  
7 the transmitting antenna of an interrogator, the signal present on node  
8 "A" of Fig. 29 becomes large. For example, the signal on node "A"  
9 could be several hundreds of millivolts. The rising and falling edges  
10 of the detected signal are controlled by two separate time constants  
11 which are very different, as shown in Fig. 31. As shown by the high  
12 power signal of Fig. 31, the high power signal has a rising edge which  
13 is fast, or has a very steep, nearly vertical slope. The nearly vertical  
14 slope of the rising edge results because the rising edge is controlled by  
15 the effective resistance of the Schottky diode (about 1 kOhm) multiplied  
16 by the capacitance of capacitor 90 (Crf) (about 1-10pF). Hence, the  
17 resulting time constant is about 1 to 10 nanoseconds.

18 In contrast, the falling edge of the detected signal in Fig. 31 is  
19 controlled by the current source 88 as it discharges capacitor 90 (Crf),  
20 which takes approximately 100 nanoseconds. As a result, the voltage  
21 waveform at node "A" is distorted. According to the amplified digital  
22 version of the signal, shown in Fig. 31, the signal in the high power  
23 case is distorted by the unequal rise and fall times. The onset of each  
24 fall for the digital version is triggered at the cross-over point, which

1 deviates substantially from that of the low power signal. Such a  
2 distortion poses a serious problem for implementing clock recovery  
3 schemes, which rely on accurate edge-to-edge timing.

4 To overcome the above-mentioned problem, the integrated  
5 circuit 16 of Fig. 6 uses only rising edges for clock recovery. Hence,  
6 the distorted falling edges are avoided altogether. As becomes apparent  
7 from viewing the amplified digital signal of Fig. 31, rising edge to rising  
8 edge timing is not affected by the slow falling edges. Therefore, the  
9 clock can be accurately recovered.

10 Fig. 30 illustrates a circuit 93 including a Schottky diode  
11 detector 94, and an antenna 44 connected to the Schottky diode  
12 detector 94. More particularly, in the illustrated embodiment, the  
13 Schottky diode detector 94 includes a Schottky diode 96 having a  
14 cathode connected to the antenna 44 and an anode. The Schottky  
15 diode detector 94 further includes a current source 98 driving current  
16 in the direction from the anode to the cathode of the Schottky  
17 diode 96 and through the antenna 44. The Schottky diode detector 94  
18 further includes a capacitor 100 connected between the anode of the  
19 Schottky diode 96 and ground; and a capacitor 102 connected between  
20 the anode of the Schottky diode 96 and an output of the diode  
21 detector 94 which is connected to an amplification circuit. The same  
22 technique used with respect to Fig. 29 can also be implemented for the  
23 Schottky diode detector circuit of Fig. 30. However, for this case, only  
24 the rising edges are significantly distorted, since the Schottky diode is

reversed in direction. Therefore, only the falling edges are used in clock recovery.

#### Details of Method of Forming an IC Schottky Structure

A method of forming a Schottky structure that can be employed to manufacture the Schottky diode detector will now be described. A Schottky diode is a diode in which a metal and a semiconductor form a pn junction. Electrons injected into the metal have a higher energy level than the charge carriers in a semiconductor, and energy storage at the junction is low because current flow is not accompanied by hole movement.

One embodiment of the invention comprises a Schottky diode 220 including an n+ region 222 generally encircling or surrounding an n-well region 224 (Fig. 41). In the illustrated embodiment, the n+ region 222 is heavily doped; e.g.,  $1 \times 10^{18}$  atoms/cm<sup>3</sup> or greater of n-type material, and the n-well region 224 is lightly doped; e.g.,  $1 \times 10^{17}$  atoms/cm<sup>3</sup> or lower of n-type material. The n-well region 224 defines a contact area 226, and the n+ region 222 provides a low resistance interconnect to the Schottky diode 220. The n+ region 222 has a diffused edge 228, and the n-well region has a contact edge 230. The distance from the n+ region diffused edge 228 to the n-well region contact edge 230 is minimized. In one embodiment, the distance from the n+ region diffused edge 228 to the n-well region contact edge 230 is less than twenty micrometers. In a more preferred embodiment, the distance

1 from the n+ region diffused edge 228 to the n-well region contact  
2 edge 230 is about two micrometers.

3 More particularly, the integrated circuit 16 includes a grid pattern  
4 of n+ regions 222. Each region 222 generally encircles or surrounds  
5 isolated n-well regions 224 of a large common n-well region 232 under  
6 the n+ regions 222 (Figs. 41 and 42). This provides for parallel  
7 connection of a selectable number of Schottky diodes 220. As described  
8 elsewhere, the parallel connection of Schottky diodes 220 acts a single  
9 Schottky diode, and allows use of standard sized contact holes. The  
10 number of Schottky diodes 220 connected together is selectable to tailor  
11 resistance, parasitic capacitance, and electrostatic discharge sensitivity for  
12 a specific application.

13 To form the grid of Schottky diodes 220, the following process  
14 steps are performed.

15 First, a p- substrate 234 is provided (Fig. 38). Next, n-well  
16 region 232 is defined relative the substrate 234. Next, an insulator 236  
17 is formed over the n-well region. In one embodiment, the insulator 236  
18 is borophosphosilicate glass (BPSG).

19 Next, a removal or etching step is performed to remove areas of  
20 the insulator 236 for definition of contact holes 238, and areas 240  
21 generally encircling or surrounding the contact holes 238 (Fig. 39). The  
22 contact holes 238 are not necessarily circular in cross-section; any cross-  
23 sectional shape is possible. Similarly, any cross-sectional shape is  
24 possible for the areas 240 surrounding the contact holes 238. In a

1 preferred embodiment, the contact holes 238 all have the same diameter  
2 (or peripheral extent) to facilitate subsequent filling of the contact  
3 holes 238 (described below in greater detail). In an alternative  
4 embodiment, different contact holes 238 have different sizes. In the  
5 process of the illustrated embodiment, the contact holes 238 do not  
6 need to be completely filled with a conductor, and all contact holes  
7 therefore do not need to be the same size.

8 In the illustrated embodiment, the n+ regions 222 are formed in  
9 the n-well region 232 by diffusion after the etching has been performed,  
10 via the openings 240 surrounding the contact holes 238. The n+  
11 regions 222 can be formed by other processes or in other sequences.  
12 For example, the n+ regions 222 can be formed before the  
13 insulator 236 is formed over the n-well region 232.

14 Next, a Schottky forming metal 242 such as titanium is formed in  
15 the contact hole openings. In the illustrated embodiment, the Schottky  
16 forming metal is deposited on the surface of n-well regions 224 via the  
17 contact hole openings 238. In one embodiment, the thickness of the  
18 deposited metal is about 200 Å. The metal is annealed to form a  
19 stable silicide interface to the n-well silicon.

20 If it is desired to fill the contact holes, a material such as  
21 tungsten 246 may be deposited into the contact holes (Fig. 40). The  
22 tungsten is then planarized to form final contact structures (Fig. 41).

23 Then, an interconnect metallization step is performed (Fig. 42).  
24 For example, copper doped aluminum 248 is deposited (e.g. sputtered)



1 over the wafer, then the wafer is masked and etched to remove  
2 unwanted areas. The mask defines a pattern to interconnect the  
3 contacts as desired.

4 A variable number of Schottky diodes may be connected in  
5 parallel by simply changing the metal masks and interconnecting only  
6 the number of Schottky diodes required by a particular circuit  
7 application. In one illustrated embodiment, an array of twelve by  
8 twelve Schottky diodes (144 total Schottky diodes) is provided (Fig. 43).  
9 In another embodiment (Fig. 42), less than all available Schottky diodes  
10 are connected together. In one embodiment, only a six by six array  
11 (36 Schottky diodes) is connected together in parallel.

12 In one alternative embodiment, aluminum is employed instead of  
13 tungsten and silicide. In another alternative embodiment, tungsten is  
14 employed instead of aluminum to interconnect contacts, and the step of  
15 forming tungsten plugs is omitted.

16 In an alternative embodiment (Fig. 47), each Schottky diode  
17 includes a p+ region 252 encircling a "p-" p-well region 254 and is  
18 formed by a method substantially identical to the method described  
19 above except with p-type material substituted for n-type material and  
20 vice versa. More particularly, in this alternative embodiment, the  
21 following steps are performed.

22 First, an n-type substrate 256 is provided (Fig. 44). Next, a  
23 common p-well region 258 is defined relative the substrate 256. The  
24 common p-well region 258 defines the p-well regions 254 for each of

1 the Schottky diodes. Next, an insulator 260 such as borophosphosilicate  
2 glass (BPSG) is formed over the p-well region 258. Next, an etching  
3 step is performed to etch away regions of the insulator for definition  
4 of contact holes, and areas 264 generally encircling or surrounding the  
5 contact holes (Fig. 45). In a preferred embodiment, the contact  
6 holes 262 all have the same diameter (or peripheral extent) to facilitate  
7 subsequent filling of the contact holes 262 with Tungsten or another  
8 conductor. In an alternative embodiment, different contact holes 262  
9 have different diameters. In the process of the illustrated embodiment,  
10 the contact holes do not need to be completely filled, and all contact  
11 holes therefore do not need to be the same size.

12 In the illustrated embodiment, the p+regions 252 are formed in  
13 the p-well regions by diffusion after the etching has been performed,  
14 via the openings 264 encircling the contact holes. The p+regions 252  
15 can be formed by other processes or at other times. For example, the  
16 p+regions 252 can be formed before the insulator is formed over the  
17 p-well region 258.

18 Next, a Schottky forming metal 266 such as Titanium is formed  
19 in the contact hole openings 262. In the illustrated embodiment, the  
20 Schottky forming metal 266 is deposited on the surface of the p-well  
21 region 258 via the contact hole openings 262. In one embodiment, the  
22 thickness of the deposited metal is about 200 Å. The metal 266 is  
23 annealed to form a stable silicide interface 268 to the p-well region  
24 258.

1 If it is desired to fill the contact holes 262, a metal such as  
2 tungsten 270 is deposited into the contact holes (Fig. 46). The  
3 tungsten 270 is then planarized to form final contact structures.

4 Then, an interconnect metallization step is performed (Fig. 47).  
5 For example, copper doped aluminum 272 is deposited (e.g. sputtered)  
6 over the wafer, then the wafer is masked and etched to remove  
7 unwanted areas. The mask defines a pattern to interconnect the  
8 contacts as desired.

9 The above described processes for forming a Schottky diode are  
10 preferred over a process wherein, after the contact holes are etched, ion  
11 implantation of phosphorus into the holes is performed. In such a  
12 process, the implant would be a two step process, with a low energy  
13 implant (e.g., 35 keV of  $4 \times 10^{12}$  ions/cm<sup>2</sup>) followed by a high energy  
14 implant (e.g., 120 keV of  $4 \times 10^{12}$  ions/cm<sup>2</sup>). Such implants cause a high  
15 doping level at the bottom of the contact hole, which prevents  
16 formation of a low leakage Schottky diode. The preferred processes  
17 described above eliminates these two contact implants, and allows for  
18 formation of a good quality Schottky diode.

19 Figs. 8.0101AA-CB provide a circuit drawing of the Schottky diode  
20 detector "diodedet." Figs. 8.0101AA-CB actually show two Schottky  
21 diode detectors. The lower Schottky diode detector shown in Figs.  
22 8.0101AA-CB is a replicated or dummy detector which generates a  
23 signal for the complement side of the differential amplifier "videoamp1."  
24 The structure of the dummy Schottky diode detector is similar to the

real Schottky diode detector so that any noise coupled through ground or possibly through Vdd is replicated on both sides of the differential amplifier "videoamp1" and so that the common mode rejection of the amplifier will result in little noise making it through the amplifier chain. Bias current to the Schottky diode detector is provided by the current source transistors having gates connected to "BIAS1" and "BIAS2" respectively. A path for that current is through the antenna. Thus, the antenna is biased to a high potential Vdd. The array of capacitors in Figs. 8.0101AA-CB is a series capacitance that couples the output of the Schottky detector to the input of the video amp "videoamp1" and allows an independent bias level to be set at the input of the video amp "videoamp1." The value of that capacitor in conjunction with the effective resistance seen looking into the amplifier "videoamp1" determines the high pass response of the amplifier "videoamp1." The values of the capacitor and effective resistance determine the lowest frequency at which the amplifiers can respond, and that frequency is selected to be low enough so that none of the information contained in the base band signal is lost.

Figs. 8.0102AA-BD provide a circuit drawing of the CMOS detector "cmosdet" which is employed in an alternative embodiment.

#### Details of Quick Bias AC-Coupled Video Amplifier

Fig. 48 provides a simplified circuit schematic of a quick bias AC-coupled video amplifier 270. The video amplifier goes from a power

1 down (unbiased) state to a fully biased state quickly despite a large  
2 value effective resistance and capacitor used to bias and couple the  
3 amplifier.

4 The video amplifier 270 has an input adapted to be connected to  
5  $V_{in}$  and includes coupling capacitors 292 and 294 at the input.

6 The video amplifier includes a voltage divider 276 including two  
7 resistors 278 and 280 in series, and four transistors 282, 284, 286,  
8 and 288 shown to the right of a voltage divider in Fig. 48.  
9 Transistors 286 and 288, the rightmost two of the four transistors, are  
10 long L (length), narrow W (width) p-channel devices operated in linear  
11 mode to provide very high effective resistance  $R_{EFF}$ . Transistors 286  
12 and 288 are used instead of resistors because it is hard to provide high  
13 resistances using resistors without generating undesirable parasitic  
14 capacitance and without taking up more space on an integrated circuit  
15 die. The video amplifier 270 includes a differential amplifier 290. The  
16 voltage divider 276 sets a bias voltage at the inputs of the differential  
17 amplifier 290. The effective resistance  $R_{EFF}$ , in conjunction with the  
18 value of coupling capacitor 292 or 294, sets the angular high pass roll  
19 off frequency for the amplifier according to a relationship of  
20  $\omega_{HP} = 1 / ((R_{EFF} + R1 || R2) C1)$  where  $\omega$  is angular frequency ( $2\pi$  times  
21 frequency), R1 and R2 are the values of the resistors 278 and 280  
22 included in the voltage divider 276, and C1 is the value of one of the  
23 coupling capacitors. The values of  $R_{EFF}$ , and the coupling capacitors  
24 are adjusted to achieve the desired high pass roll off frequency  $\omega_{HP}$  as

1 illustrated in Fig. 49. The high pass roll off frequency determines what  
2 frequencies will be amplified or attenuated. The high pass roll off  
3 frequency is set low enough so that important data is not excluded.

4 In many applications, the values of these components are high.  
5 For example, in the integrated circuit 16,  $R_{EFF}$  is approximately two  
6 MegaOhms, and the capacitance of each of the coupling capacitors 292  
7 and 294 is approximately one picoFarad, which gives an angular high  
8 pass frequency of approximately  $1/((2\text{MegaOhms})(1\text{pF}))=500$   
9 kiloradians/second, or a high pass frequency of  $500/2\pi=79.6$  kHz.

10 In a powered down state, input  $V_{reg}$  is zero. Upon power up,  
11 there is a delay before the inputs reach the desired bias voltage,  
12 according to a relationship  $V_{BIAS}=R1/(R1+R2)V_{reg}$ . The time constant  
13 equals  $R_{EFF}C1$  which is approximately equal to two microseconds.

14 If it is decided to wait five time constants, this requires about ten  
15 microseconds.

16 In accordance with the invention, transistors 282 and 284 are  
17 added (the two leftmost transistors of the four). These are short L  
18 (length) wide W (width) devices which allow the bias voltage to be  
19 established in much less time by shorting around the high resistance of  
20 the right two transistors 286 and 288. The time constant is thereby  
21 reduced. This shorting occurs when an input RXEN is low. Before  
22 using the circuit as an amplifier, RXEN is taken high (after bias  
23 voltage is achieved). This restores the desired frequency behavior.  
24

1 Figs. 8.0103AA-CF provide a circuit drawing of the video amp  
2 "videoamp1." The video amp "videoamp1" is a differential amplifier  
3 with a cascode device isolating a resistor load from differential  
4 transistors of the amplifier. This lowers capacitance and improves the  
5 frequency response of the amplifier. Bias is provided by a resistor  
6 divider shown on the upper left of Figs. 8.0103AA-CF, which resistor  
7 divider provides a potential to two p-channel transistors found almost  
8 in the center of the Figs. 8.0103AA-CF. Each of these p-channel  
9 transistors defines a very large resistance, effectively on the order of  
10 one to two megaOhms connecting to the nodes of the amplifier to  
11 provide the bias. The remaining p-channel devices shown left of center  
12 in Figs. 8.0103AA-CF are shorting devices which short out the two  
13 p-channel transistors during the period when the receiver is being  
14 powered on out of the sleep mode. The function of these remaining  
15 p-channel devices is to cause the inputs to the receiver to come up to  
16 the bias level as quickly as possible. They are then shut off in order  
17 to leave the circuit with only the high resistance p-channel devices  
18 providing the bias. This is necessary from a frequency response  
19 standpoint.

20 Figs. 8.0104AA-BC provide a circuit drawing of the video amp  
21 "videoamp2." The video amp "videoamp2" operates in a manner similar  
22 to operation of the video amp "videoamp1." The video amp  
23 "videoamp1" has a higher bias current than the video amp "videoamp2."  
24 The reason for this is to minimize the noise generated in the amplifier.

1 Figs. 8.0105AA-EE provide a circuit drawing of the comparator  
2 "comparator." The comparator has biasing considerations similar to the  
3 biasing considerations for the video amps, and has a biasing network  
4 shown at the left in Figs. 8.0105AA-EE, at the inputs, which is similar  
5 to the biasing networks in the video amps. The function of the  
6 comparator "comparator" is to ensure an output at a full digital level.

7 Figs. 8.0106AA-CD provide a circuit drawing of an RF detect  
8 circuit "rxdet." This circuit generates an RF detect signal. The circuit  
9 includes an input switch that is either high or low, and a capacitor.  
10 If the input switch is high for a sufficient percentage of the time, the  
11 input switch will charge up the capacitor. The capacitor has a  
12 continual discharge leakage current. As long as the input switch is high  
13 sufficiently frequently, the input switch will overcome the capacitor  
14 leakage current, and the circuit "rxdet" will put out an RF detect  
15 signal.

16 Figs. 8.0107AA-GN provide a circuit drawing showing construction  
17 details of the receiver bias generator "rxbias." The receiver bias  
18 generator includes a series of current mirrors to produce bias currents  
19 for various stages of the receiver.

20 Figs. 8.0108AA-AC provide a circuit drawing showing construction  
21 details of a data transition detector "datatx." The data transition  
22 detector has an input connected to the digital level output of the  
23 comparator "comparator" of the receiver "rx" in Figs. 8.01AA-DE. The  
24 data transition detector generates a high going pulse every time there



1 is a transition from high to low or from low to high in the data  
2 output by the comparator "comparator." These transitions are tested  
3 by other circuitry, described below, to determine whether or not a valid  
4 signal is being received.

#### 5 6 Details of Low Power Frequency Locked Loop

7 As previously discussed, the integrated circuit 16 periodically  
8 checks if a radio frequency signal is being received by the receiver.  
9 The integrated circuit 16 includes a timer setting the period for the  
10 checking, the timer comprising a frequency locked loop "lpfll."

11 The low power frequency locked loop "lpfll" is shown in greater  
12 detail in Figs. 8.02AA-BC. This is also shown in a simplified schematic  
13 in Fig. 24. In the embodiment shown in Fig. 24, the device 12  
14 includes a frequency locked loop (or phase locked loop) 54, a  
15 divider 55 coupled to the input of the loop 54, and a divider 56  
16 coupled to the output of the loop 54. A clock (e.g. 9.54 MHz) that  
17 is recovered from an incoming radio frequency command from the  
18 interrogator 26 is supplied to the frequency locked loop (or phase  
19 locked loop) 54 after being passed through the divider 55. The terms  
20 "phase locked loop" or "frequency locked loop" as used herein are  
21 meant to describe physical structure, not a state of operation. The  
22 term "locked" does not imply that the circuitry is operating, or  
23 functioning in a locked condition. Thus, as used herein, "locked" is a  
24 term for assisting definition of a particular circuit configuration and is

not meant to imply a required state of operation for the circuit. To avoid ambiguity, the appended claims use the terms "phase lock loop" or "frequency lock loop" instead of "phase locked loop" or "frequency locked loop" to indicate that state of operation is not being claimed.

Phase locked loops and frequency locked loops are similar to one another, except that a phase locked loop tracks phase as well as frequency. A phase locked loop includes a phase detector having a first input receiving the incoming message, having a second input, and having an output; a loop filter having an input coupled to the output of the phase detector and having an output; a voltage controlled oscillator having an input coupled to the output of the loop filter, and having an output defining an output of the phase locked loop; and a divider having an input coupled to the output of the voltage controlled oscillator and having an output connected to the second input of the phase detector. The phase detector produces an output voltage proportional to the phase difference of two input signals. The loop filter is used to control the dynamics of the phase locked loop. The voltage controlled oscillator produces an AC output having a frequency proportional to input control voltage. The divider produces an output signal having a frequency that is an integer division of the input signal. The loop filter includes a capacitor on a control node of the voltage controlled oscillator.

The frequency locked loop 54 includes a frequency comparator 57 receiving the divided recovered clock, an up/down counter 58 connected

1 to the output of the frequency comparator, and a current controlled  
2 oscillator 59 connected to the output of the up/down counter. The  
3 output of the current controlled oscillator 59 is fed back to the  
4 frequency comparator 57, and to the divider 56. The divider 56 is  
5 programmable (in response to a radio frequency command from the  
6 interrogator 26) in one embodiment of the invention. To conserve  
7 power, the loop 54 is enabled only during processing of a command  
8 from the interrogator 26, during which time a recovered clock reference  
9 signal is available. In the illustrated embodiment, the current controlled  
10 oscillator 59 is a low power current controlled oscillator "lpcco" shown  
11 in Figs. 8.0204AA-EJ.

12 Figs. 8.02AA-BC provide a circuit drawing of the low power  
13 frequency locked loop "lpfl." This circuit generates a clock which is  
14 used in multiple places to time the interval between wake ups. The  
15 clock is used as a reference for the timed lock out function, and for  
16 the alarm timer wake up function. In a preferred embodiment, the low  
17 power frequency locked loop "lpfl" generates a 8 kHz clock. The low  
18 power frequency locked loop includes a current controlled oscillator  
19 "lpcco" that consumes very little current and that runs continuously from  
20 the time power is first supplied to the integrated circuit 16 ("power  
21 up") until power is removed from the integrated circuit 16. During  
22 power up, the low power frequency locked loop "lpfl" attempts to  
23 synchronize to the main clock recovery oscillator "dcr" (described below).  
24 However, that oscillator is not calibrated to anything yet because it has

just been powered on. Still, an initial frequency is set for the low power frequency locked loop "lpfl." On the first successful communication with an interrogator, the low power frequency locked loop "lpfl" is actually calibrated to a known clock frequency and set to a desired frequency (8 kHz in the illustrated embodiment).

The low power frequency locked loop includes a divider shown at the top of Figs. 8.02AA-CB. The divider divides down an input clock signal. In the illustrated embodiment, the input clock signal is a 9.5 MHz clock signal. The input clock signal is divided down by a desired factor to get a reference clock for the actual loop shown at the bottom of Figs. 8.02AA-CB. In the preferred embodiment, the reference clock for the loop shown in Figs. 8.02AA-CB runs at 8 kHz. The loop receives a loop enable signal "LoopEN", shown at the lower left of Figs. 8.02AA-CB. The loop enable signal "LoopEN" enables this frequency locked loop to operate in a loop configuration. The loop enable signal "LoopEN" is asserted when a valid message has been certified and on power up. Those are the only two times the loop enable signal is asserted.

The frequency of the current controlled oscillator "lpcco" is determined by current input into the current controlled oscillator "lpcco." A selection of the number of current steps for controlling the oscillator is made by the outputs of the up/down counter "udcounter." The up/down counter has outputs select 1 "Sel1," select 2 "Sel2," select 4 "Sel4," and select 8 "Sel8." The outputs of the up/down counter are

1 labelled according to their binary weights, and that is also how currents  
2 are rated within the current controlled oscillator. When the loop is  
3 disabled, at the end of processing of a valid command, the count on  
4 the output of the up/down counter is frozen so that the select 1  
5 through select 8 lines remain constant and they keep that same  
6 frequency in the low power frequency locked loop "lpfl" until the next  
7 valid command is processed. At the time when the next valid command  
8 is processed, if the clock frequency of the low power frequency locked  
9 loop has drifted, the loop sets the frequency back to the desired  
10 frequency (e.g., 8 kHz).

11 Figs. 8.0201AA-AB provide a circuit drawing showing construction  
12 details of a timed lockout divider cell "tldcel\_bypass" included in the  
13 circuit of Figs. 8.02AA-BC.

14 Figs. 8.0202AA-CD provide a circuit drawing of a frequency  
15 comparator "freqcomp" of the frequency locked loop "lpfl." The  
16 frequency comparator counts a certain number of cycles of the  
17 reference clock and also counts how many cycles of the low power  
18 clock occurred within that number of cycles. The frequency comparator  
19 thus determines whether the low power clock "lpfl" is running too fast,  
20 too slow, or on time. If the clock is running too fast or too slow, the  
21 frequency comparator makes an adjustment by causing the counter  
22 "udcounter" to either count up or count down. If no adjustment is  
23 necessary, the frequency comparator makes no adjustment to the  
24 counter.

Figs. 8.0203AA-BC provide a circuit drawing showing construction details of the up/down counter "udcounter" included in the low power frequency locked loop "lpfl." The counter has some logic on the counter's output so that if the counter counts all the way down to zero, the counter does not wrap around and go to all ones. Instead, the counter stops at zero (until a signal requesting an up count is received). Similarly, if the counter counts all the way up to all ones, the counter does not wrap around to all zeros. Instead, the counter stops at all ones (until a signal requesting a down count is received).

Figs. 8.020301AA-BB provide a circuit drawing showing construction details of an adder “udcounter\_adder” included in the up/down counter.

Figs. 8.020302AA-AB provide a circuit drawing showing construction details of a D type flip-flop “udcounter\_dff” included in the up/down counter.

### Details of Low Power Current Controlled Oscillator

The integrated circuit 16 includes the low power current controlled oscillator "lpcco." The oscillator consumes very little current (e.g., less than 100 nA). The oscillator "lpcco" includes digital input lines, and oscillates at a frequency controlled by the digital input lines. The circuit includes a thermal generator, a digitally controlled current mirror, an oscillator, and an output driver.

Figs. 8.0204AA-EJ provide a circuit drawing of the low power current controlled oscillator "lpcco." The low power current controlled

oscillator "lpcco" includes a thermal voltage generator, including a string of resistors, shown in Figs. 8.0204AA-EJ in the upper left corner. The thermal voltage generator generates a small voltage proportional to  $kT/q$  across the string of resistors where  $k$  is Boltzmann's constant,  $1.38 \times 10^{-23}$  Joules per degree Kelvin,  $T$  is temperature in degrees Kelvin, and  $q$  is the electron charge in Coulombs. The voltage  $kT/q$  is approximately equal to 26 mV at room temperature. That small voltage divided by the resistor value sets the current in the circuit. This current is approximately equal to  $(kT/qR) \ln ((W/L)Q1)/(W/L)Q2)$ . In the illustrated embodiment, the current is set to a low value (e.g., approximately three nano-amps).

Thermal generators are known in the art. See for example, "CMOS Analog Integrated Circuits Based on Weak Inversion Operation" by Eric Vittoz and Jean Fellrath, IEEE Journal of Solid-State Circuits, Vol. SC-12, No. 3, June 1977. See particularly Fig. 8 of this article, and the associated description.

The low power current controlled oscillator "lpcco" also includes a wake up circuit shown to the far left of the thermal voltage generator that causes a much higher current to flow initially to turn on the feedback loop. The wake up circuit then shuts off and leaves the low value (nano-amp) current flowing. Thus, initialization occurs on power up and the wake up circuit is off after that unless power is removed and reapplied. The outputs of the up/down counter "udcounter," select 1 "Sel1," select 2 "Sel2," select 4 "Sel4," and select

1 8 "Sel8" come into the low power current controlled oscillator as shown  
2 on the left edge of Figs. 8.0204AA-EJ. The low power current  
3 controlled oscillator further includes control circuitry shown on the  
4 bottom strip of Figs. 8.0204AA-EJ. These outputs of the up/down  
5 counter control the number of currents that are mirrored into this  
6 control circuitry by a current mirror. The current mirror is digitally  
7 controlled and weightings are binary in the illustrated embodiment;  
8 however, any weighting scheme can be used. The current mirror  
9 includes transistors operating in the subthreshold, or weak inversion  
10 mode, due to the extremely low current level.

11 More particularly, referring to Figs. 8.0204AA-EJ, there are five  
12 transistors to the right of the string of resistors, mirrored down to one  
13 about the center of the page providing a divide by five. Current is  
14 then mirrored through all the p-channel devices. The block shown in  
15 the upper right of Figs. 8.0204AA-EJ is a selectable current mirror.  
16 The first stage generates one current equal to the reference current and  
17 that is always flowing into the n-channel diode down at the bottom of  
18 that stack. Shown to the right of the n-channel diode are the  
19 selectable groups of p-channels. The first one has one, the next two,  
20 the next four, the next eight in a binary sequence. The transistors  
21 shown below the p-channels transistors are select devices and they are  
22 controlled by the digital signals select 1 "Sel1," select 2 "Sel2," select  
23 4 "Sel4," and select 8 "Sel8." Thus, the number of currents can be  
24



1 selected and however many are selected are added into the one that  
2 is always flowing in the diode.

3 The current from groups of p-channel transistors that are not  
4 selected is diverted over to a separate or second diode shown on the  
5 far right of Figs. 8.0204AA-EJ. This is so that when a block of  
6 transistors is not selected, their drain nodes do not get pulled up to  
7  $V_{DD}$ . By sinking the current in this second diode, the voltage at the  
8 drain node of an unselected block of transistors is kept down near the  
9 voltage at which it will operate when and if it is actually connected  
10 over to the first diode. This is so that, upon switching a select line,  
11 a capacitance doesn't have to be charged from  $V_{DD}$  down to the  
12 proper operating voltage. In any case, the selected number of currents  
13 are added together into the first diode, and then that voltage is carried  
14 on the line shown in Figs.8.0204AA-EJ as going down the right side of  
15 page, which line has a capacitor tied to it. That capacitor is a filter  
16 capacitor so that the voltage on that node does not change abruptly  
17 when the select lines change or when some unrelated signal nearby  
18 switches. Since all of these transistors are operating in a sub-threshold  
19 or weak inversion mode, a small change in the voltage on their gate  
20 will otherwise result in a rather large impact on the operation of the  
21 circuit. That line is the input for the circuitry shown across the  
22 bottom of Figs.8.0204AA-EJ. There is a current mirror situation there,  
23 so that the sum of all the selected currents plus the one default  
24 current flowing in the diode above is mirrored and flows through the

1 p-channel devices of this circuitry. There is then another mirror to  
2 generate bias voltages for the n-channel current source devices for the  
3 VCO ring oscillator. The p-channel gate voltages are used in mirroring  
4 into the p-channel load devices of the same ring oscillator. The  
5 frequency of this ring oscillator is controlled by the current mirrored to  
6 them.

7 The low power current controlled oscillator includes a four stage  
8 ring oscillator. The frequency of oscillation is approximately  
9 proportional to the amount of current flowing. The frequency of  
10 oscillation of the four stage ring oscillator is directly proportional to its  
11 bias current over a wide range of frequencies. For example, frequency  
12 is directly proportional to bias current for frequencies between  
13 approximately 100 Hz and tens of MHZ (e.g. to twenty MHZ).

14 The low power current controlled oscillator further includes an  
15 output driver. In the illustrated embodiment, the output driver includes  
16 a comparator circuit receiving the output of the fourth stage ring. The  
17 purpose for this comparator is to convert the small output signal of the  
18 oscillator to full digital levels. In the illustrated embodiment, full digital  
19 levels are zero volts and  $V_{DD}$ . In the illustrated embodiment,  $V_{DD}$  is  
20 3.3 Volts  $\pm 0.3$  Volts. In an alternative embodiment,  $V_{DD}$  is 5 Volts  
21  $\pm 10$  or 20%. Another other suitable values can be employed for  $V_{DD}$   
22 and the digital levels.

23 Circuitry is included to eliminate the crossover current in the n  
24 and p channel devices in the first few invertors. This is because, when

1 operated at very low current levels, the rise and fall times are long and  
2 could allow substantial current to flow in the n and p channel devices  
3 during switching.

4 The digital levels are buffered and amplified up by the  
5 comparator to provide an output signal from the low power frequency  
6 locked loop "lpfl." The output of the low power current controlled  
7 oscillator is shown on the right edge of Figs. 8.0204AA-EJ. In the  
8 illustrated embodiment, the low power current controlled oscillator  
9 operates at eight kHz. However, if desired for alternative embodiments,  
10 the low power current controlled oscillator is capable of running at a  
11 frequency from approximately 100 Hz to 20 kHz. In an alternative  
12 embodiment, the low power current controlled oscillator is capable of  
13 running at a frequency from approximately 100 Hz to 30 kHz.

14 The low power current controlled oscillator consumes very little  
15 power. For example, in the illustrated embodiment, the low power  
16 current controlled oscillator consumes less than a milliAmp. More  
17 particularly, in the illustrated embodiment, the low power current  
18 controlled oscillator consumes approximately 100 nanoAmps.

19 In an alternative embodiment, instead of using a thermal voltage  
20 generator, a transistor is biased in the subthreshold region in order to  
21 define the current source and to generate a small current. However,  
22 in this embodiment, the voltage on the gate of the transistor is updated  
23 periodically as it leaks away.  
24

1 Although the low power current controlled oscillator has been  
2 described in connection with a radio frequency identification device, the  
3 low power current controlled oscillator can be advantageously employed  
4 in any battery powered electronic product which must keep track in  
5 time.

6 Figs. 8.03AA-AB provide a circuit drawing showing construction  
7 details of a counter bit "lpfl\_cbit" included in the receiver "rx."

8 Figs. 8.04AA-EE provide a circuit drawing of the wake up  
9 controller "rxwu." An input to the wake up controller is a clock signal  
10 "LPCLK" from the low power frequency locked loop "lpfl." This clock  
11 signal input is shown in the upper left of Figs. 8.04AA-EE. The clock  
12 signal "LPCLK" is further divided down to provide certain time  
13 intervals available for selection. These are the time intervals at which  
14 the integrated circuit 16 will wake up and look for a radio frequency  
15 signal. In the illustrated embodiment, these time intervals are set at  
16 0.5, 16, 64 and 256 milliseconds. The selection of one of these  
17 multiple available time intervals is accomplished via radio frequency  
18 command from the interrogator.

19 The wake up controller includes wake up abort logic shown in the  
20 lower left of Figs. 8.04AA-EE. The wake up abort logic performs a  
21 number of tests (described elsewhere herein) to determine whether the  
22 received signal is a valid signal and, if all tests are passed, then the  
23 wake up controller asserts a signal on line "RXWU" shown on the right  
24

1 of Figs. 8.04AA-EE. This signal wakes up the processor, and the  
2 processor then processes the command contained in the message.

### 3 4 Details of Wake Up Tests

5 Figs. 8.0401AA-AB provide a circuit drawing of a wake up abort  
6 logic circuit "wuabort." The wake up abort logic circuit provides for  
7 conservation of battery power. If what is received is not a valid  
8 message, the wake up abort logic circuit determines this quickly and the  
9 device returns to the sleep mode so that the battery is not drained on  
10 invalid messages or spurious communication. The wake up abort logic  
11 circuit works by counting clock cycles. The wake up abort logic circuit  
12 has as an input a clock signal "CHIPCLK" that is the output of the  
13 clock recovery oscillator "dcr" (described below). This clock signal is  
14 divided down by a factor of four, which results in a value  
15 approximately equal to the spread spectrum chip rate. After the clock  
16 is actually acquired from a message from the interrogator, the resulting  
17 value will be equal to the chip rate.

18 Initially though, when these wake up tests are performed, a clock  
19 has not yet been acquired from a message. The wake up abort logic  
20 includes an RF Detect Timer, shown on the top, left of Figs. 8.0401AA-  
21 EE, which performs a first test. The RF Detect Timer counts a  
22 predetermined number of cycles of the clock (e.g., 13 cycles) and, if the  
23 RF detect signal from the receiver is not asserted, the wake up is  
24 aborted. On the other hand, if the RF detect signal is asserted within

1 those cycles, the wake up abort logic starts the next series of tests  
2 without waiting for the end of the predetermined number of cycles.

3 The next series of tests are timed by a counter shown across the  
4 center of the page in Figs. 8.0401AA-EE. For the next tests,  
5 transitions in the incoming data stream are counted within a certain  
6 time interval and the number of transitions must fall within a certain  
7 range in order to pass the test. Transitions are counted by the counter  
8 shown at the bottom in Figs. 8.0401AA-EE. The range limits are set  
9 by knowing the number of transitions that should occur in the data  
10 within the amount of time allowed. This is known because each data  
11 bit is encoded as a thirty-one chip sequence as described elsewhere  
12 herein. The reason there is a range is because the clock has not yet  
13 been acquired accurately so there is a range of clock frequencies that  
14 must be considered. In the illustrated embodiment, one test checks  
15 whether, after five counts of the clock, there has been between greater  
16 than or equal to one, and less than eight transitions in the data. If  
17 not, the wake up is aborted and the device goes back to sleep. If yes,  
18 then the next test is performed.

19 The next test checks whether, after twenty-six clock counts, there  
20 are greater than or equal to fourteen and less than thirty-two transitions  
21 in the data. If not, wake up is aborted and the chip goes back to the  
22 sleep mode. If this test is passed, the wake up abort logic circuit  
23 performs tests relating to signals generated by the clock recovery nodes.  
24 One such test is a test for chip lock. Chip lock is an indication that

1 clock recovery is proceeding and has actually gotten within a few  
2 percent of the desired clock frequency. The final check is whether  
3 frequency lock has occurred. Again, these tests are timed. If one of  
4 the signals is not asserted by the time the timer signal goes high, then  
5 the wake up will be aborted and the device goes back to sleep and  
6 will try again after another wake up interval. Frequency lock will come  
7 into the logic in the center of the page in Figs. 8.04AA-CB, and that  
8 is what causes the RXWU signal to be asserted, thus waking up the  
9 processor.

10 Another function of the wake up abort logic shown in Figs.  
11 8.0401AA-EE is to discriminate between high rate and low rate. The  
12 wake up abort logic measures time while these tests are performed to  
13 determine when the interrogator is in high rate, but the chip is in low  
14 rate or vice versa and abort out of wake up (return to the sleep  
15 mode).

16 These tests will now be described in connection with flowcharts  
17 illustrated in Figs. 25-27.

18 The wake up controller "rxwu" was described above in connection  
19 with Figs. 8.04AA-EE. The wake up tests performed by the wake up  
20 controller are illustrated in flow chart form in Figs. 25-26.

21 When the integrated circuit 16 first wakes up, bias generators and  
22 the receiver "rx" are powered on (step S1 in Fig. 25). After ensuring  
23 that the bias is on (step S2 in Fig. 25), the master clock "dcr" is  
24 started. By design, the master clock "dcr" starts at a frequency below

1 the final frequency it will achieve after the clock recovery circuit "lpfl"  
2 extracts the clock frequency from the incoming signal. More  
3 particularly, in the illustrated embodiment, the master clock starts at a  
4 start frequency above half of the final frequency it will achieve after  
5 the clock recovery circuit "lpfl" extracts the clock frequency from the  
6 incoming signal. Still more particularly, in the illustrated embodiment,  
7 the master clock starts at a start frequency between half and three  
8 quarters of the final frequency the master clock will achieve after the  
9 clock recovery circuit "lpfl" extracts the clock frequency from the  
10 incoming signal. In the illustrated embodiment, the final frequency is  
11 38.15 MHZ, and the start frequency is between 20 and 30 MHZ. The  
12 master clock includes a frequency locked loop including a voltage  
13 controlled oscillator. An offset is applied to the oscillator to make  
14 sure that the clock starts at least as fast as 20 MHZ. Then, the  
15 frequency locked loop adjusts the frequency to 38.15 MHZ.

16 Because the clock has not yet been acquired from the incoming  
17 signal, the clock is a free running oscillator when providing the start  
18 frequency. Initial wake up tests are performed at this lower start  
19 frequency. The receiver "rx," digital clock and data recovery circuit  
20 "dcr," pseudo random number processor "pnproc," and voltage controlled  
21 oscillator "vco" are turned on (step S3 in Fig. 25).

22 The input radio frequency signal received from the interrogator 26  
23 is a direct sequence spread spectrum input signal in the illustrated  
24 embodiment. Spread spectrum techniques are described above. In one



embodiment, incoming radio frequency commands are included in packets that contain, in order of transmission, a preamble, a Barker code, and the command. In one embodiment, each bit of the incoming radio frequency command sent by the interrogator is modulated using a pseudo noise (PN) sequence for direct sequence spread spectrum communication.

After the clock is running, the device 12 is in a receiver on mode illustrated in Fig. 27 by a vertical line marked "WAKEUP RX ON." After the clock is running, the device 12 performs wake up tests (at the lower or start frequency).

A first test is whether the receiver "rx" detects any radio frequency signal within a predetermined number of clock cycles (step S4 in Fig. 25). In the illustrated embodiment, this predetermined number of clock cycles is 13. If no radio frequency signal is detected by the receiver "rx" within 13 clock cycles, the device 12 returns to the sleep mode. If a radio frequency signal is detected by the receiver "rx" within 13 clock cycles, the device 12 switches to a wake up abort test mode illustrated in Fig. 27 by a vertical line marked "WAKEUP ABORT TESTS," and a second test is performed.

In the second test, a determination is made as to whether a predetermined number of data transition pulses occur within a predetermined number of clock pulses for the radio frequency signal detected by the receiver "rx" (step S5 in Fig. 25). More particularly, the device 12 includes a long counter shown in Figs. 8.0401AA-EE

1 driven by a clock signal "CHIPCLK." The device 12 further includes  
2 a circuit "datatx" which detects transitions in the signal received by the  
3 receiver "rx" and generates a pulse ("DTX" in Fig. 26) at each  
4 transition. The device 12 further includes another counter circuit shown  
5 in Figs. 8.0401AA-EE which counts these pulses. Because a valid  
6 incoming signal is modulated with a known PN sequence, the number  
7 of transitions in a given time for a valid incoming signal is known.  
8 The device 12 includes logic "wuabort" that tests whether the proper  
9 number of data transition pulses occur within a certain number of clock  
10 pulses. More particularly, in the illustrated embodiment, the logic tests  
11 whether more than or equal to one and less than eight such data  
12 transition pulses occur within five chips. If not, the device returns to  
13 the sleep mode. If so, a third test is performed.

14 In the third test, a determination is made as to whether a  
15 predetermined number of data transition pulses occur within a  
16 predetermined number of clock pulses for the radio frequency signal  
17 detected by the receiver "rx" (step S5 in Fig. 26). The third test is  
18 similar to the second test, except that the number of data transition  
19 pulses is tested against a number of clock pulses that is different from  
20 the number in the second test. More particularly, in the illustrated  
21 embodiment, the logic tests whether more than or equal to fourteen and  
22 less than thirty-two such data transition pulses occur within thirty-one  
23 chips. If not, the device 12 returns to the sleep mode.  
24

1 If the above transition tests are passed, the device 12 checks to  
2 see if the clock recovery circuit locks onto the incoming clock rate.  
3 More particularly, in the illustrated embodiment, a determination is  
4 made as to whether a clock is acquired from the incoming signal within  
5 6k chips (step S7 in Fig. 26). A determination is then made as to  
6 whether frequency lock is achieved within 16k chips (step S9 in Fig.  
7 26). The device 12 returns to the sleep mode if any of these tests  
8 fail. If these tests are passed, then the device 12 enters a processor  
9 on mode illustrated in Fig. 27 by a vertical line marked "PROCESSOR  
10 ON." Power is supplied to the processor (step S10 in Fig. 26) and the  
11 device 12 waits for the preamble of the incoming message to end and  
12 the command to begin.

13 In one embodiment, the tests of Fig. 26 are employed to  
14 distinguish between incoming signals with different possible valid chipping  
15 rates.

16 More particularly, in the illustrated embodiment, it is known how  
17 long each of the various tests should take for valid low chipping rate  
18 or high chipping rate signals, and this information can be tested to  
19 determine whether the incoming signal is a high rate or low rate signal.

20 Other appropriate tests can be performed in embodiments where  
21 spread spectrum is not employed. In these embodiments, knowing how  
22 valid data is encoded, the wake up timer and logic still compares the  
23 number of transitions received in a given amount of time with an  
24 expected number of transitions for a valid signal.

1 Figs. 8.040101AA-AB provide a circuit drawing showing construction  
2 details of a counter bit "wuabort-cbit" included in the wake up abort  
3 logic.

4 Figs. 8.0402AA-AB provide a circuit drawing showing construction  
5 details of a timed lockout divider cell "tldcel" included in the receiver  
6 wake up controller.

### 7 8 Details of Lock Detection in a Digital Clock Recovery Loop

9 In many communications systems, it is necessary to recover a  
10 clock signal from the received data. A phase locked loop is one way  
11 of recovering such a clock signal. In the illustrated embodiment, such  
12 a recovered clock is used as a master clock.

13 The integrated circuit 16 includes the digital clock and data  
14 recovery circuit "dcr" which includes a phase locked loop. The phase  
15 locked loop includes a voltage controlled oscillator "dcr\_vco." The  
16 frequency of the voltage controlled oscillator always starts low, at  
17 between 50% and 75% of the final desired value. When the voltage  
18 controlled oscillator starts running, large steps are taken (Fig. 54). As  
19 the frequency approaches the final value, increasingly smaller steps are  
20 taken to achieve greater accuracy. The illustrated embodiment employs  
21 four step sizes: large, medium, medium-fine, and fine. For example, in  
22 the illustrated embodiment, large steps up are employed between 50%  
23 to 75% of the final desired value, and medium steps up are then taken  
24 above 75% until pump up commands are not issued for a

1 predetermined number of transitions, then medium-fine steps up are  
2 employed until the final value is overshoot, then fine steps down are  
3 employed.

4 A method is needed to determine when the frequency of the  
5 voltage controlled oscillator matches the desired frequencies contained  
6 in the received data.

7 The voltage controlled oscillator includes a control node having  
8 a voltage indicative of the frequency of the voltage controlled oscillator.  
9 The behavior of this node is used to determine when frequency lock  
10 has occurred.

11 After the phase locked loop has run long enough to get within  
12 a few percent of the final value (at a time illustrated as  $T_0$  in  
13 Fig. 54), a signal "SDD" (start data decoding) is generated. This signal  
14 "SDD" disables the large and medium steps and enables lock detect  
15 circuitry for determining if frequency lock has occurred. A latch  
16 "KILLSU" (kill start up) detects when the first fine step pump down  
17 occurs (at  $T_1$  in Fig. 54). This enables a latch "FREQLOCK." The  
18 latch "FREQLOCK" is set when the first fine step pump up occurs (at  
19 a time illustrated as  $T_2$  in Fig. 54). A signal "FREQLOCK" is then  
20 indicative that the phase locked loop has reached its final value.

21 In other words, large, medium, then medium-fine steps up are  
22 followed by fine steps down. The final value is overshoot, and a  
23 frequency lock signal is provided upon occurrence of the first  
24 subsequent fine step up.

1 In the illustrated embodiment, the final value of the voltage on  
2 the control node of the voltage controlled oscillator, where frequency  
3 lock is expected, is approximately 1.2 Volts. In one embodiment, each  
4 large step is approximately several hundred milliVolts, each medium step  
5 has a size approximately in the tens of milliVolts (e.g., 25 milliVolts),  
6 each medium-fine step has a size of approximately a few milliVolts (e.g.  
7 two milliVolts), and each fine step has a size approximately in the  
8 tenths of milliVolts. Various other relative sizes or numbers of steps  
9 are employed in alternative embodiments.

10 The sizes of steps is set using current sources of different values  
11 that are turned on for a fixed period of time to drive to the capacitor  
12 on the control node of the voltage controlled oscillator.

13 In the illustrated embodiment, the fine step generator is not  
14 disabled before time  $T_0$  so there is a possibility that a combination of  
15 fine steps with larger steps can take place before time  $T_0$ . In an  
16 alternative embodiment, however, the fine step generator is disabled  
17 before time  $T_0$ .

18 Figs. 8.05AA-CB provide a circuit drawing of the digital clock and  
19 data recovery circuit "dcr." The digital clock and data recovery circuit  
20 includes a phase locked loop of a digital design, and a state machine  
21 "dcr\_statemachine" that drives the phase locked loop. The phase locked  
22 loop includes a voltage controlled oscillator "dcr\_vco" and control  
23 circuitry "dcr\_vcocontrol" for the voltage controlled oscillator. The  
24 voltage controlled oscillator "dcr\_vco" includes a control node ("OUTN")

1 and "OUTP" shown in Figs. 8.0504AA-EE and described below in  
2 greater detail) and produces an oscillation at a rate dependent on the  
3 value of a voltage applied to the control node. In the illustrated  
4 embodiment, the state machine has four states. The phase locked loop  
5 produces an output pulse on a line "OUTC" (later labeled  
6 "FMASTER"). The digital clock and data recovery circuit attempts to  
7 place four pulses of the output clock within one chip time.

8 The state machine "dcr\_statemachine" determines when that is not  
9 the case and, if not, whether to cause the oscillator to run faster or  
10 to run slower. The state machine "dcr\_statemachine" then issues  
11 appropriate pump up or pump down signals to drive a control node of  
12 the oscillator. The voltage controlled oscillator "dcr\_vco" starts out at  
13 a minimum frequency as determined by an offset current which is  
14 present regardless of the loop. This ensures that the oscillator will  
15 start up and run at greater than 50% of the final value so that the  
16 phase locked loop will converge on the proper frequency. The digital  
17 clock and data recovery circuit also includes a PLL start-up circuit  
18 "dcr\_startup." The acquisition of the clock frequency happens in stages  
19 and, initially, the control node moves in large increments towards its  
20 final value. The start-up circuit "dcr\_startup" provides large increments  
21 for controlling the loop. However, as the digital clock and data  
22 recovery circuit gets closer to acquisition of clock frequency, control  
23 switches from that start up circuit "dcr\_startup" over to the state  
24 machine "dcr\_statemachine." The state machine provides very fine steps

1 as the final convergence is done with very fine steps. The data stream  
2 is fed into the circuitry on the upper right. Then the data is sampled  
3 during one of the states of the state machine after it has been  
4 determined that the data is valid. The data stream is recreated and  
5 called "RXCHIPS."

6 Figs. 8.0501AA-BE provide a circuit drawing of the start up circuit  
7 "dcr\_startup" included in the digital clock and data recovery circuit. In  
8 the illustrated embodiment, the start up circuit provides either very  
9 large or fairly large steps dependent upon how far from frequency the  
10 oscillator is running. The start up circuit also has a counter (shown  
11 along the bottom in Figs. 8.0501AA-BE) that determines when there  
12 have been no pump up commands issued for a given count of  
13 transitions. In the illustrated embodiment, the counter determines when  
14 there have been no pump up commands during sixteen transitions. If  
15 the given count of transitions are detected in the data and there has  
16 been no pump up command (e.g., no pump up medium or pump up  
17 fast command) then a signal is asserted on a line "SDD." SDD stands  
18 for Start Data Decode and is an indication that the control voltage has  
19 converged to within a few percent.

20 Figs. 8.050101AA-BE provide a circuit drawing showing construction  
21 details of a shift register cell "dcr\_sreg" included in the PLL start up  
22 circuit. Figs. 8.050102AA-AB provide a circuit drawing showing  
23 construction details of a counter bit "dcr\_counterbit" included in the  
24 PLL start up circuit.



1 Figs. 8.0502AA-CD provide a circuit drawing of the state machine  
2 "dcr\_statemachine." In the illustrated embodiment, the state machine  
3 has four states. The state machine includes two flip-flops with feedback  
4 signals providing the four states. This circuit generates pump up slow,  
5 and pump down slow commands for adjusting voltage on a control node  
6 of the voltage controlled oscillator.

7 This circuit also has the circuitry that turns off the start up  
8 circuit and generates the frequency lock signal. When trying to acquire  
9 frequency lock, there will be large and medium pump ups, without any  
10 pump downs, until the final desired value is overshoot. At this point,  
11 there will be a first pump down slow pulse. When the first pump  
12 down slow command is issued, the start up circuitry "dcr\_startup" is  
13 turned off, which leaves only fine step capability for adjustment in the  
14 control voltage. It takes time for the fine steps to bring down the  
15 control node voltage to the proper value and the voltage on the control  
16 node will overshoot the desired voltage in the negative direction. The  
17 state machine will detect that it has gone too far and it will step the  
18 voltage back up towards the final value and that first fine step up will  
19 be detected and at that point the frequency lock signal is asserted.

20 Figs. 8.0503AA-BB provide a circuit drawing of a bias generator  
21 "dcr\_bias." The bias generator includes current mirrors that generate  
22 the appropriate bias values for the various circuits in the digital clock  
23 and data recovery block.  
24

1 The digital clock and data recovery circuit "dcr" includes a VCO  
2 control voltage generator "dcr\_vcocontrol" which is shown in greater  
3 detail in Figs. 8.0504AA-EE.

4 The digital clock and data recovery circuit "dcr" employs a phase  
5 locked loop to recover the clock frequency from an incoming radio  
6 frequency message. Phase locked loops use feedback to maintain an  
7 output signal in a predetermined phase relationship with a reference  
8 signal.

#### 9 10 Details of Digital Clock Recovery Loop

11 Operation and design of the digital clock and data recovery circuit  
12 "dcr" will now be further described with reference to Figs. 61-72

13 In many communications systems it is necessary to recover a clock  
14 signal from the received digital data stream. In the device 12, this  
15 clock signal is used as the master timing reference to eliminate the  
16 need for an external crystal-based timing reference. Typically, a phase  
17 locked loop of some type is used to extract the clock.

18 There are many requirements on the phase locked loop used to  
19 recover a clock signal from the received digital data stream. Several  
20 important ones for this application are that the phase locked loop must  
21 acquire the desired frequency without locking to a multiple or sub-  
22 multiple of the desired frequency; the phase locked loop must lock to  
23 the desired frequency within a certain time of interest; and the phase  
24 locked loop must yield consistent performance despite wide variation in

1 device parameters which is inherent in integrated circuit processing.  
2 The phase locked loop employed in the illustrated embodiment,  
3 embodied in the digital clock recovery circuitry "dcr," satisfies all of  
4 these requirements.

5 In the illustrated embodiment, the forward link baseband data is  
6 encoded for direct sequence spread spectrum. In the illustrated  
7 embodiment, a data bit "1" is represented by a thirty-one chip sequence  
8 and a data bit "0" is represented by the logical inversion of the same  
9 thirty-one chip sequence.

10 The mode of operation of the device 12 is as follows. The chip  
11 periodically awakens from a low-current sleep mode in order to detect  
12 whether  
13 an incoming RF message is present. The clock recovery loop "dcr" is  
14 inactive in the low-current sleep mode. If a message is present, the  
15 message is tested to make sure it is a valid message from an  
16 interrogator. If the incoming signal passes these tests, the clock  
17 recovery loop is enabled, the clock is acquired, the message is  
18 processed, and a reply is sent. The device 12 then returns to sleep  
19 mode.

20 The digital clock recovery loop is illustrated by reference numeral  
21 700 in Fig. 61. The digital clock recovery loop 700 comprises several  
22 sub-circuits. The digital clock recovery loop 700 includes a voltage  
23 controlled oscillator 702. The voltage controlled oscillator 702 has an  
24 output 704, and produces a square wave at output 704 having a

frequency controlled by the voltage on an input control node. When the voltage on the control node is zero, the frequency at output 704 is at least one half of the final recovered frequency and not greater than the final recovered frequency. The output frequency rises monotonically, nearly linearly, as the control node voltage is increased. This is shown in Fig. 62. More particularly, Fig. 62 illustrates the frequency produced at the output 704 of the voltage controlled oscillator 702 relative to a voltage at the input control node.

The digital clock recovery loop 700 further includes a charge pump and loop filters which control the rate of change of the voltage on the control node of the voltage controlled oscillator. The charge pump and loop filters are designated in Fig. 61 with reference numeral 706.

The digital clock recovery loop 700 further includes a start-up circuit 708 which performs frequency detection when the voltage controlled oscillator first starts up and, in conjunction with the charge pump and loop filters 706, causes the voltage on the control node of the voltage controlled oscillator to change rapidly.

The digital clock recovery loop 700 further includes a state machine 710 which performs phase detection when the frequency of the voltage controlled oscillator is within a few percent of its final value and, in conjunction with the charge pump and loop filters, causes the voltage on the control node of the voltage controlled oscillator 702 to change slowly.

1 The only analog blocks are the voltage controlled oscillator 702  
2 and the charge pump. The rest of the circuits of the digital clock  
3 recovery loop are digital circuits which are easy to build at high yield  
4 in integrated circuit processes.

5 In the preferred embodiment, the voltage controlled oscillator 702  
6 is the voltage controlled oscillator "dcr\_vco" shown in the detailed  
7 schematic drawings, and has control nodes "OUTN" and "OUTP"; the  
8 state machine 710 is the state machine "dcr\_statemachine" shown in the  
9 detailed schematic drawings; and the start-up circuit 708 is the start-up  
10 circuit "dcr\_startup" shown in the detailed schematic drawings.

11 The digital clock recovery loop causes the frequency at the output  
12 of the voltage controlled oscillator to vary until a predetermined number  
13 of this clock fit within the time interval of an identifiable discrete  
14 segment of the incoming data. More particularly, in the illustrated  
15 embodiment, the digital clock recovery loop causes the frequency at the  
16 output of the voltage controlled oscillator to increase until exactly four  
17 cycles of the clock fit within the time interval of a single chip. In  
18 alternative embodiments, other integer numbers could be used. In the  
19 illustrated embodiment, a state machine having four states is employed  
20 to cause the frequency at the output of the voltage controlled oscillator  
21 to increase until exactly four cycles of the clock fit within the time  
22 interval of a single chip. A general description of the behavior of the  
23 control node voltage can be found above in the section titled Details  
24 of Lock Detection in a Digital Clock Recovery Loop.

1       What follows is a discussion of the operation of each block of  
2 the digital clock recovery loop. The start-up circuit 708 is show in Fig.  
3 61. Although it may be simplified from the circuitry shown in the  
4 detailed schematics including "dcr\_startup" shown in Figs. 8.0501AA-BE,  
5 the theory of operation is the same.

6       The start-up circuit 708 includes a plurality of flip-flops 712  
7 chained together, a plurality of flip-flops 714 chained together, and an  
8 exclusive-or gate 716. The exclusive-or gate 716 has an output  
9 connected to the input of the first of the flip-flops 714, has an input  
10 connected to the output of the last of the flip-flops 712, and has  
11 another input connected to the input of the same flip-flop 712. More  
12 particularly, in the illustrated embodiment, each flip-flop 712 and 714  
13 is a D-type flip-flop and has a D input, a clock input, and a Q output.  
14 The D input of flip-flops 712 other than the first flip-flop is connected  
15 to the Q output of a previous flip-flop 712. The first flip-flop 712 is  
16 connected to the input data "Data In." The D input of flip-flops 714  
17 other than the first flip-flop 714 is connected to the Q output of a  
18 previous flip-flop 714. The first flip-flop 714 is connected to the  
19 output of the exclusive-or gate 716. The clock inputs of the flip-flops  
20 712 and 714 are all tied to the output 704 of the voltage controlled  
21 oscillator 702. Data is shifted from the D input of each flip-flop to  
22 the Q output of the same flip-flop on each clock pulse. Thus, the  
23 flip-flops 712 as a group define a shift register, and the flip-flops 714  
24 as a group define a shift register.

1 The start-up circuit 708 further includes an AND gate 718 that  
2 has one input that is the output of the exclusive-or gate 716, has a  
3 second input that is the output of the second of the flip-flops 714, and  
4 defines an output "Puf1" (a first pump up fast output). The start-up  
5 circuit 708 further includes an AND gate 720 that has one input that  
6 is the output of the exclusive-or gate 716, has a second input that is  
7 the output of the third of the flip-flops 714, and defines an output  
8 "Puf2" (a second pump up fast output).

9 The start-up circuit 708 further includes a counter 722 that  
10 receives as inputs "Puf1" and "Puf2" and generates an output "SDD"  
11 (start data decode) when the output of the voltage controlled oscillator  
12 702 is close to its final value.

13 The exclusive-or gate 716 in the center of the page generates a  
14 high output whenever there is a transition in the data as sampled by  
15 the clock signal output by the voltage controlled oscillator 702 output  
16 clock. Assume for discussion that data is latched into all flip-flops 712  
17 and 714 on the falling edge of the clock. Puf2 goes high when three  
18 falling edges of the clock occur within one chip because the inputs of  
19 the AND gate are spaced apart by three flip-flops. Three falling edges  
20 of the clock occur within one chip when the frequency is between 75%  
21 and 100% of the final value. Puf1 goes high when two falling edges  
22 of the clock occur within one chip because the inputs of the AND gate  
23 are spaced apart by two flip-flops. Two falling edges of the clock  
24 occur within one chip when the clock frequency is 50% to 75% of its

final value. This is shown on the waveform diagram of Fig. 63 for the case when the frequency is exactly 50%. Puf1 could be used to pump up the control node of the voltage controlled oscillator 702 rapidly. Puf2 could be used to pump up the control node of the voltage controlled oscillator 702 at a rate equal to that for Puf1 (as is shown in Fig. 61) or it could pump at a slower rate (as is done in the circuitry shown in the detailed schematics). As the clock frequency approaches 75% of final in the Puf1 case or 100% of final in the Puf2 case, pump up signals occur infrequently as error must accumulate over a long time to cause the appropriate number of clock edges to shift within a chip. This is used to detect when the clock frequency is close to its final value.

The counter 722 counts transition pulses until it is cleared by a Puf1 or Puf2 signal. If a predetermined large number of transitions are counted before a pump up occurs, a signal is asserted on a line SDD (start data decode). In the illustrated embodiment, if sixteen transitions are counted before a pump up occurs, a signal is asserted on line SDD. This indicates that the voltage on the control node of the voltage controlled oscillator is within a few percent of its final value, allowing data to be accurately recovered.

In the illustrated embodiment, the state machine 710 issues finer pump-up signals than the start-up circuit 708, and can also issue pump-down signals. In the illustrated embodiment, the start-up circuit 708 only issues pump up signals. The state machine 710 has as many



1 states as the number of clock cycles which fit within one chip time.  
2 In the illustrated embodiment, the state machine has four states. The  
3 state machine 710 counts clock pulses and expects the data to transition  
4 at a count of one every time there is a transition. If the transition  
5 actually occurs at a count of four then the clock is too slow and a  
6 pump up is issued. If the transition actually occurs at a count of two  
7 then the clock is too fast and a pump down is issued. If the  
8 transition actually occurs at a count of three, it is not known whether  
9 the clock is fast or slow so no adjustment is made to the voltage  
10 controlled oscillator. A state diagram is shown in Fig. 64.

11 Design of a clocked sequential circuit is known in the art. See,  
12 for example, chapter 6 of Digital Logic and Computer Design by M.  
13 Morris Mano, 1979, Prentice-Hall, Inc. A typical design procedure  
14 involves describing circuit behavior using a state diagram (see Fig. 64),  
15 obtaining a state table (see Fig. 66), assigning binary values to each  
16 state (see Fig. 64), determining the number of flip-flops needed (see  
17 Fig. 65), choosing the type of flip-flops to be used (see Fig. 65), using  
18 Karnaugh maps or other simplification methods, deriving circuit output  
19 functions and flip-flop input functions (see Figs. 67 and 68), and  
20 drawing the logic diagram. The numbers in parentheses in Fig. 64 are  
21 the binary state numbers. ENDT enables the sampling of the data  
22 (always at state two when no transition occurred). There are several  
23 ways to implement a circuit to perform functions of a state diagram.  
24 Assume that Q1 and Q0 are the binary state numbers in parentheses

above (Q1 on the left, Q0 on the right), and that D1 and D0 are the next state values of Q1 and Q0, respectively. This is illustrated in Fig. 65. The flip-flop outputs Q0 and Q1 are the states. Then, a state table can be derived. This is shown in Fig. 66. Using Karnaugh maps (see Figs. 67 and 68), minimum logic to perform the desired function can be derived. It should be noted, of course, that minimum logic need not be employed--logic involving an increased number of logic gates but performing the same desired function can also be employed. From the Karnaugh map shown in Fig. 67, the following equation can be derived:

$$D0 = Q1 + TX \cdot Q0 + En \cdot TX$$

which can also be written as:

$$D0 = [Q1' \cdot (TX \cdot Q0)' \cdot (En \cdot TX)']'$$

where the symbol "+" represents a logical OR, the symbol "'" represents a logical AND, and the symbol "" represents a logical NOT.

From the Karnaugh map shown in Fig. 68, the following equation can be derived:

$$D1 = TX' \cdot Q1 \cdot Q0' + En \cdot TX' \cdot Q0'$$

which can also be written as:

$$D1 = [(TX' \cdot Q1 \cdot Q0')' \cdot (En \cdot TX' \cdot Q0')']'$$

where the symbol "+" represents a logical OR, the symbol "'" represents a logical AND, and the symbol "" represents a logical NOT.

Logic to implement these equations is shown in Figs. 69 and 70.

Paths shown in Fig. 64 are defined as follows:

1 ENDT=Q1'Q0·TX'

2 PumpUpSlow=Q1·Q0'·TX; and

3 PumpDownSlow=Q1'·Q0·TX

4 Logic used to implement the state machine, in accordance with  
5 one embodiment of the invention, is shown in Figs. 8.0502AA-CD.

6 A simplified timing diagram showing operation of the state  
7 machine is shown in Fig. 71. The crowding and separation of states  
8 in Fig. 71 is exaggerated to show the various modes of operation in a  
9 compact form. More particularly, it is highly unlikely that a pump  
10 down signal would be necessary so soon after a pump up signal as is  
11 depicted in Fig. 71.

12 The state machine is trying to fit four cycles of the output of the  
13 voltage controlled oscillator in one chip width. Referring simultaneously  
14 to Figs. 71 and 64, starting at the first occurrence of state 3 in Fig.  
15 71, there is no transition, so the state machine will proceed to state  
16 4 on the next clock. At state 4, there is no transition, so the state  
17 machine will proceed to state 1 at the next clock. At state 1, there  
18 is a transition in the waveform. The state machine always proceeds to  
19 state 2 from state 1. At state 2, there is no transition. From state  
20 2, the state machine proceeds to state 3. This cycle is repeated and  
21 these paths are followed unless the clock recovery loop drifts off  
22 frequency.

23 If the clock recovery loop drifts off frequency, other paths of the  
24 state diagram of Fig. 64 are followed. For example, if a transition is

FIG. 8.0505AA-EF

1 seen at state 4, the voltage controlled oscillator is oscillating too slowly,  
2 and a PumpUpSlow is issued. The state machine skips state 1 and  
3 goes to state 2.

4 If, after going from state 1 to state 2, a transition is seen, the  
5 voltage controlled oscillator is oscillating too fast. The state machine  
6 will go from state 2 to state 2 so that state 2 is now in the proper  
7 position.

8 If a transition is seen at state 3, the voltage controlled oscillator  
9 may either be oscillating too fast or too slowly, so no pump up or  
10 pump down signals are issued. Instead, the state machine proceeds to  
11 state 2.

12 The control functions performed by the start-up circuit and state  
13 machines can be used to control the frequency of any voltage controlled  
14 oscillator. The particular voltage controlled oscillator 702 that is  
15 employed in the illustrated embodiment is shown in Figs. 8.0505AA-EF.

16 In the illustrated embodiment, the voltage controlled oscillator 702  
17 includes a current controlled four-stage ring oscillator shown in the  
18 center of Figs. 8.0505AA-EF. The frequency of oscillation is very much  
19 linearly proportional to the bias current flowing in each stage.

20 The voltage controlled oscillator 702 further includes an  
21 Operational Transconductance Amplifier shown on the left side of Figs.  
22 8.0505AA-EF. This Operational Transconductance Amplifier converts a  
23 voltage difference at its inputs to a current difference at its outputs.

24

1 This Operational Transconductance Amplifier has a characteristic that is  
2 linear over a range of input voltage.

3 The composite circuit is a voltage controlled oscillator 702 with  
4 nearly linear operation about the operating point of 38.15 MHz. The  
5 circuit shown to the right in Figs. 8.0505AA-EF converts the small  
6 signal output of the oscillator to full digital levels.

7 The input reference voltage is generated by a bandgap regulator  
8 and has a value of about 1.2 volts. The circuit is designed so that at  
9 nominal conditions the control node needs to pump to about equal to  
10 the reference voltage to oscillate at 38.15 MHz.

11 The start-up circuit requires that the oscillator start at greater  
12 than half frequency (approximately 19 MHz) and less than full frequency  
13 over all operating conditions and for all process variations. This  
14 oscillator start frequency is set by providing an offset current to the  
15 bias of the oscillator which is not controlled by the input voltage. In  
16 the illustrated embodiment, the range of allowed offset currents is  
17  $7.437\mu\text{A}$  to  $9.763\mu\text{A}$ . A value of  $8.2\mu\text{A}$  was chosen. Thus, the  
18 oscillator start frequency will vary from about 20 MHz to 34 MHz.

19 The charge pump and loop filters 706 are shown in greater detail  
20 in Figs. 8.0504AA-EE. The filter capacitors are shown on the right  
21 side of Figs. 8.0504AA-EE. In the illustrated embodiment, the filter  
22 capacitors include a first group of ten capacitors, defining a total  
23 capacitance of 10 pF, and an second group of ten capacitors, defining  
24 a total capacitance of 10 pF. In Figs. 8.0504AA-EE, the first group

1 of ten capacitors is shown above the second group of ten capacitors.  
2 Other values or numbers are possible. In the illustrated embodiment,  
3 the lower group of capacitors is connected to the reference voltage  
4 input to the voltage controlled oscillator 702. The upper group of  
5 capacitors is connected to the control node input of the voltage  
6 controlled oscillator 702. The control node always starts at 0 Volts and  
7 is pumped up. The other (reference) side is always at the bandgap  
8 voltage.

9 The charge pump is shown in the center of Figs. 8.0504AA-EE.  
10 In the illustrated embodiment, there are actually four charge pumps.  
11 The method employed is to steer a current to charge or discharge the  
12 10 pF capacitor for a prescribed period of time (one cycle of the  
13 recovered clock, in the illustrated embodiment). The change in control  
14 voltage for a single pump is:

$$\Delta V = (I/C) \Delta t$$

16 The lower three of the illustrated charge pumps are controlled by  
17 the start-up circuit 708 and can only pump up. The upper pump is  
18 controlled by the state machine 710 and can pump up or down in fine  
19 steps. The step sizes are controlled by the current value which is set  
20 accurately using a bandgap regulator to generate a reference current  
21 and using current mirrors to set the pump current. The step sizes  
22 used in the illustrated embodiment are shown in Fig. 72. Of course,  
23 other step sizes can be employed, as desired, and various numbers of  
24 different sized steps can be employed.

1 The time used for the calculations for the coarse and medium  
2 cases is 40 ns, a typical value for the starting period of the oscillator.  
3 26.2 ns is used for the medium fine and fine cases because these steps  
4 occur when the oscillator is close to its final frequency.

5 The course and medium steps are controlled by the Puf1 and  
6 Puf2 outputs of the start-up circuit. More particularly, in the illustrated  
7 embodiment, the course steps are controlled by the PumpUpFast output  
8 of the start-up circuit "dcr\_startup" shown in the detailed schematic  
9 drawings, and the medium step is controlled by the PumpUpMed output  
10 of the start-up circuit "dcr\_startup" shown in the detailed schematic  
11 drawings. The medium fine step is also controlled by the PumpUpMed  
12 signal but the step size is reduced when the SDD (start data decode)  
13 signal is asserted indicating the oscillator is within a few percent of its  
14 final value. The fine step is controlled by the state machine and is  
15 used to "close in" on the final value.

16 While this charge pump and loop filter configuration is  
17 advantageous for implementation on an integrated circuit, other  
18 configuration are possible. For example, simple RC filters can be  
19 employed.

#### 20 21 Details of Transmit Frequency Derivation from Incoming Data

22 The illustrated embodiment has a loop filter including capacitors  
23 on respective control nodes "OUTN" and "OUTP" (shown in Figs.  
24 8.0504AA-EE) of the voltage controlled oscillator "vco." In the

illustrated embodiment, the loop filter capacitor on the control node "OUTP" is defined by a plurality of capacitors in parallel, and the loop filter capacitor on the control node "OUTN" is defined by a plurality of capacitors in parallel. The voltage on the respective control nodes is indicative of the frequency at which the voltage controlled oscillator "vco" is oscillating. After an entire incoming message has been received by the receiver "rx," the control nodes and the capacitors on the control nodes are isolated from driving circuitry. The control voltage is thus stored in analog form on the capacitors, and the voltage controlled oscillator "vco" continues to oscillate at the recovered frequency. The length of time that the voltage stored on the capacitors is valid depends on leakage currents that can charge or discharge the capacitors over time.

In the illustrated embodiment, such leakage currents are minimized by minimizing n+ and p+ active areas on the control node, and by minimizing drain to source voltages on devices connected to the control nodes. The values for the respective capacitors are chosen, in conjunction with loop filter requirements, to hold the control voltages for as long as possible as required before the device 12 transmits a reply to the received radio frequency command. This amount of time is approximately several hundred milliseconds in the illustrated embodiment.

The output frequency of the voltage controlled oscillator can be multiplied up to generate a carrier frequency for the transmitter, as



1 described elsewhere, or can be divided down to generate tones for FSK  
2 (frequency shift keyed) transmission or DPSK (differential phase shift  
3 keyed) transmission depending<sup>4</sup> on what form of transmission is selected  
4 for the transmitter "tx."

5 In one embodiment, only one control node is employed; however,  
6 in the illustrated embodiment, a differential control node scheme is  
7 employed involving two control nodes "OUTN" and "OUTP." Therefore,  
8 in the illustrated embodiment, a capacitor is provided on each control  
9 node, and control voltages are stored in analog form on these two  
10 capacitors.

11 Figs. 8.0504AA-EE provide a circuit drawing of the control voltage  
12 generator "dcr\_vcocontrol." The control voltage generator shows the  
13 control nodes for the voltage controlled oscillator. The control voltage  
14 generator is a differential circuit. The control nodes are shown on the  
15 right edge of Figs. 8.0504AA-EE as "OUTP" and "OUTN," where  
16 "OUTN" is actually tied to the band gap voltage, which is approximately  
17 1.2 Volts. "OUTP" is the node that is pumped up to adjust frequency.  
18 The control voltage generator includes step size generators shown on the  
19 left half of Figs. 8.0504AA-EE. The steps are achieved by conducting  
20 a current to the capacitor on the control node for a prescribed length  
21 of time. For a large step, a large current is applied to this capacitor.  
22 For a small step, a smaller current is applied to this capacitor. The  
23 capacitor on the control node "OUTP" is defined by ten capacitors in  
24 parallel in the illustrated embodiment.

1 A similar capacitor, defined by ten capacitors in parallel, is  
2 provided on the other control node "OUTN."

3 Four different size currents are generated by fine, medium fine,  
4 medium, and coarse step generators "dcr\_finestepgen,"  
5 "dcr\_medfinestepgen," "dcr\_medstepgen," and "dcr\_coarsestepgen"  
6 respectively. The currents are either steered to the control capacitor  
7 on the control node or away from the capacitor, depending on whether  
8 there is a pump up or pump down command.

9 Figs. 8.050401AA-CK provide a circuit drawing showing construction  
10 details of the coarse step generator "dcr\_coarsestepgen." The coarse  
11 step generator includes a plurality of current mirrors.

12 Figs. 8.050402AA-CJ provide a circuit drawing showing construction  
13 details of the medium step generator "dcr\_medstepgen." The medium  
14 step generator includes a plurality of current mirrors.

15 Figs. 8.050403AA-BI provide a circuit drawing showing construction  
16 details of the medium fine step generator "dcr\_medfinestepgen." The  
17 medium fine step generator includes a plurality of current mirrors.

18 Figs. 8.050404AA-BB provide a circuit drawing showing construction  
19 details of a fine step controller "dcr\_finestepctrl."

20 Figs. 8.050405AA-EJ provide a circuit drawing showing construction  
21 details of the fine step generator "dcr\_finestepgen."

22 Figs. 8.0505AA-EF provide a circuit drawing of the voltage  
23 controlled oscillator "dcr\_vco." The voltage controlled oscillator  
24 "dcr\_vco" is a four stage ring oscillator with differential stages. The

1 voltage controlled oscillator includes an OTA (operational  
2 transconductance amplifier) shown on the left side of Figs.  
3 8.0505AA-DE. The OTA gives a linear relationship between the voltage  
4 differential at its inputs and the current at its output. The voltage  
5 controlled oscillator further includes current mirrors which mirror the  
6 current at the output of the OTA to drive the voltage controlled  
7 oscillator to change its frequency. The previously discussed control  
8 nodes ("OUTN" and "OUTP" of Figs. 8.0504AA-EE) are shown coming  
9 in on the left side Figs. 8.0505AA-DE, labelled as "INN" and "INP."  
10 The voltage controlled oscillator further includes, at its output, a  
11 comparator type circuit that provides digital levels for the output of the  
12 voltage controlled oscillator "dcr\_vco."

13 Fig. 8.0506AA-AB provide a circuit drawing of a clock generator  
14 "dcr\_rxclkgen." Different frequencies are needed for different functions.  
15 The clock generator provides outputs at different frequencies. For  
16 example, the clock generator provides an output "PROCCLK" (for the  
17 processor), an output "CHIPCLK" (chip clock); and outputs "PLLCLKP"  
18 and "PLLCLKN" for the clock that drives the state machine. The  
19 clock generator "dcr\_rxclkgen" has an input "LOWRATE" for low rate  
20 which is a signal indicative that the chip is in low rate and can expect  
21 data to come in at a chip rate of one-half the normal chip rate. The  
22 loop is adjusted in a manner such that the frequency of "FMASTER"  
23 does not change regardless of whether the chip is in high rate or low  
24 rate. However, the clock "CHIPCLK" for the integrated circuit 16 is

1 half as fast in low rate, and it takes twice as long to get data in as  
2 it would to get the same amount of data in at the high rate.

3 Fig. 8.050601 provides a circuit drawing showing construction  
4 details of a flip-flop "dcr\_rxclkgenff" included in the clock generator.

5 Figs. 8.0507AA-AB provide a circuit drawing of a non-overlapping  
6 clock generator "dcr\_clkgen." The non-overlapping clock generator  
7 receives as inputs true and compliment clock signals "ClkInP" and  
8 "ClkInN" and provides buffered true and compliment clock signals  
9 "ClkOut" and "ClkOutN." The non-overlapping clock generator buffers  
10 the true and compliment clock signals "ClkInP" and "ClkInN" in such  
11 a way that before "ClkOut" can go high, "ClkOutN" must be low, and  
12 then at the end of that cycle, before "ClkOutN" can go high, "ClkOut"  
13 must be low. Any overlap between the two clocks occurs when they  
14 are both low. They are never both high at the same time. This is  
15 quite commonly required in many circuits throughout the integrated  
16 circuit 16 where shift register type techniques are used, and one stage  
17 passes information to another. Non-overlapping clocks are required for  
18 such functions.

19 The circuit of Figs. 6AA-EK further includes a transmitter "tx."  
20 The transmitter "tx" is capable of transmitting using different modulation  
21 schemes, and the modulation scheme is selectable by the interrogator.  
22 More particularly, if it is desired to change the modulation scheme, the  
23 interrogator sends an appropriate command via radio frequency. The  
24 transmitter can switch between multiple available modulation schemes

1 such as Frequency Shift Keying (FSK), Binary Phase Shift Keying  
2 (BPSK), Direct Sequence Spread Spectrum, On-Off Keying (OOK),  
3 Amplitude Modulation (AM), and Modulated Backscatter (MBS).

4 The output responses are included in packets that contain, in  
5 order of transmission, a preamble, a Barker code, and the reply data.

6 In one embodiment, each bit of the radio frequency reply sent by  
7 the device 12 is modulated using a pseudo noise (PN) sequence for  
8 direct sequence spread spectrum communication. The sequence is  
9 generated in part by a linear feedback shift register "pngshr" having a  
10 plurality of registers "pngsreg." In one embodiment, the linear feedback  
11 shift register is in the form [5,2] which means that the input to the  
12 first register is the result of combining the output of the fifth register  
13 by the exclusive-OR with the output of the second register. This  
14 produces thirty-one states. In one embodiment, the linear feedback shift  
15 register is in the form [6,1] for a sixty-three chip sequence. In another  
16 embodiment, the linear feedback shift register is in the form [8,4,3,2]  
17 for a two hundred and fifty-five chip sequence. In a preferred  
18 embodiment, the shift register is selectable between multiple of the  
19 above forms. In the form [6,1], the input to the first of six registers  
20 is the result of combining the output of the sixth register by exclusive-  
21 OR with the output of the first register. In the form [8,4,3,2], the  
22 input to the first of eight registers is the result of combining the  
23 outputs of registers eight, four, three, and two by exclusive-OR. The  
24 sixty-three chip output sequence requires less time for signal

1 synchronization than the two hundred and fifty-five chip sequence.  
2 However, the two hundred and fifty-five chip output sequence provides  
3 better performance in systems having poor signal to noise ratio.

4 Figs. 8.06AA-ED provide a circuit drawing of the transmitter "tx."  
5 Figs. 8.06AA-ED show a transmitter PLL "txpllfsyn," a test mode data  
6 selector "txdatasel," a BPSK modulation driver "txbpsk," a frequency  
7 doubler "txdoubler," a second frequency doubler "txdoubler2," a  
8 transmitter power amp "txpoweramp," a transmitter bias generator  
9 "txbias," and a modulated backscatter transmitter "txmbs." Figs. 8.06AA-  
10 ED actually shows two different transmitters. Much of Figs. 8.06AA-ED  
11 illustrates circuitry employed for an active transmitter which is used in  
12 accordance with an alternative embodiment of the invention, but not in  
13 accordance with the preferred embodiment. Figs. 8.06AA-ED also  
14 illustrate the modulated backscatter transmitter "txmbs" that is employed  
15 in a preferred embodiment. The active transmitter will be discussed  
16 first.

17 In embodiment where the active transmitter is employed, the  
18 active transmitter operates by taking the "FMASTER" clock that was  
19 recovered from the incoming data stream and using a phase locked loop  
20 "txpllfsyn" (an analog phase locked loop in the illustrated embodiment)  
21 to multiply up the frequency. In the illustrated embodiment, the  
22 frequency is multiplied up by a factor of sixteen from 38 MHZ to 610  
23 MHZ. The phase locked loop includes an oscillator that generates  
24 eight phases which are 45° out of phase with respect to each other.







1 N times the frequency of the reference signal, where N is equal to the  
2 division factor of the divider. For the exemplary embodiment described  
3 above, N is equal to sixteen and the output frequency of the voltage  
4 controlled oscillator "txvco" is equal to sixteen times the frequency of  
5 the reference signal, e.g.  $16 \times 38.15 \text{ MHz} = 610.45 \text{ MHz}$ . By providing  
6 various output taps distributed along a ring topology of the voltage  
7 controlled oscillator "txvco," output signals of different phase  
8 relationships (but of equal frequency) are obtained from the voltage  
9 controlled oscillator "txvco." In a preferred embodiment, eight separate  
10 output taps from the voltage controlled oscillator "txvco" provide eight  
11 different output signals having substantially  $45^\circ$  differences in phase  
12 therebetween, e.g.,  $0^\circ$ ,  $45^\circ$ ,  $90^\circ$ ,  $135^\circ$ ,  $180^\circ$ ,  $225^\circ$ ,  $270^\circ$ , and  $315^\circ$ . Thus,  
13 in the illustrated embodiment, the voltage controlled oscillator "txvco"  
14 generates eight phases spaced  $45^\circ$ .

15 Figs. 8.060101AA-BB provide a circuit drawing showing construction  
16 details of the phase/frequency detector "txpfdet." The phase/frequency  
17 detector puts out a pump up signal "PU" or pump down signal "PD",  
18 and drives the charge pump.

19 Figs. 8.060102AA-BB provide a circuit drawing showing construction  
20 details of the charge pump "txchgump." The charge pump drives the  
21 loop filter.

22 Figs. 8.060103AA-CB provide a circuit drawing showing construction  
23 details of the loop filter "txloopfilter."  
24

1 Figs. 8.060104AA-DC provide a circuit drawing showing  
2 construction details of the transmitter voltage controlled oscillator  
3 "txvco." The voltage controlled oscillator "txvco" generates eight phases  
4 spaced 45°.

5  
6 Details of CMOS High Frequency VCO Stage

7 The voltage controlled oscillator "txvco" comprises a ring oscillator  
8 having four stages. Fig. 32 is a simplified schematic illustrating one  
9 stage 104. Four such stages are connected in a chain, with the outputs  
10 of the chain connected to the inputs of the chain, to define the ring  
11 oscillator. The stage 104 includes a p-channel transistor 105 having a  
12 gate defining a control node "V control," having a source connected to  
13 a supply voltage "V+," and having a drain; and a p-channel transistor  
14 106 having a gate connected to the control node "V control," having  
15 a source connected to the supply voltage "V+," and having a drain.  
16 The stage 104 further includes an n-channel transistor 107 having a gate  
17 defining an input "IN P," a drain connected to the drain of the  
18 transistor 105 and defining a node "B," and a source; and an n-channel  
19 transistor 108 having a gate defining an input "IN N," a drain  
20 connected to the drain of the transistor 106 and defining a node "A,"  
21 and a source. The stage 104 further includes an ideal current  
22 source 109 connected to the sources of the transistors 107 and 108 and  
23 directing current from the sources of the transistors 107 and 108 to  
24 ground. The stage 104 further includes a resistor 110 connected

1 between the voltage "V+" and the drain of the transistor 107, and a  
2 resistor 111 connected between the voltage "V+" and drain of the  
3 transistor 108. The stage 104 further includes a source follower 112  
4 including an n-channel transistor 113 having a gate connected to the  
5 node "A," having a drain connected to a supply voltage. "V+," and  
6 having a source defining an output "OUT P"; and an ideal current  
7 source 114 connected to the source of the transistor 113 and directing  
8 current from the source of the transistor 113 to ground. The stage 104  
9 further includes a source follower 115 including an n-channel transistor  
10 116 having a gate connected to the node "B," having a drain connected  
11 to the supply voltage "V+," and having a source defining an output  
12 "OUT N"; and an ideal current source 117 connected to the source of  
13 the transistor 116. A source follower is a circuit where the signal at  
14 the source terminal of a transistor is approximately equal to the signal  
15 at the gate of the transistor. The source followers 112 and 115 are  
16 provided in the stage 104 to provide the necessary drive for the outputs  
17 "OUT P" and "OUT N" to drive a load. More particularly, the  
18 outputs "OUT P" and "OUT N" drive amplifiers that drive frequency  
19 doublers described elsewhere herein. Nodes "A" and B" are connected  
20 to another stage in the chain (e.g., by connecting the nodes "A" and  
21 "B" to inputs "IN P" and "IN N" of a subsequent stage).

22 The ideal current source 109 drives a current "IBIAS," and the  
23 values of the resistors 110 and 111 and of "IBIAS" are chosen such  
24 that transistors 107 and 108 are in saturation. More particularly, the

1 values of the resistor 110 and the current "IBIAS" are chosen such that  
2 the value of the resistance of resistor 110 multiplied by the current  
3 "IBIAS" is less than a maximum voltage (e.g. 800 mV) to cause  
4 saturation of transistor 107. In the illustrated embodiment, resistors 110  
5 and 111 have the same resistance value. The resistors 110 and 111 are  
6 made from n-well, n+, p+, or polysilicon depending on the process  
7 used to manufacture the integrated circuit 16. Parasitic capacitance on  
8 nodes A and B is minimized by compact arrangement of the  
9 components of the stage 104. Computer software, such as from  
10 Cadence, can also be employed to reduce parasitic capacitance.

11 The stage 104 provides a differential amplifier capable of switching  
12 at a very high frequency. The switching frequency is adjustable by  
13 adjusting the voltage at control node "V control." More particularly,  
14 as the voltage at the control node "V control" decreases, the p-channel  
15 transistors 105 and 106 become more conductive, and there is less  
16 impedance between the supply voltage "V+," and the drains of the  
17 transistors 107 and 108. This provides for a faster switching rate.  
18 There is a linear change in frequency versus the voltage at the control  
19 node "V control" for at least some range of voltages.

20 Figs. 8.06010401AA-DC provide a circuit drawing showing  
21 construction details of a stage "txvcostage" included in the transmitter  
22 voltage controlled oscillator. Fig. 8.0601040101 is a layout plot showing  
23 how the components of the stage 104 of Fig. 32 are laid out. More  
24 particularly, Fig. 8.0601040101 actually shows four stages. Fig.

FIG. 8.06010501AA-AB

8.0601040101 shows locations 400 defining resistors; a line 402 providing VREG (V+ of Fig. 32); locations 404 defining source followers of Fig. 32; a location 406 defining input "IN P" of Fig. 32; a location 408 defining input "IN N" of Fig. 32; locations 410 defining the n-channel differential pair and the current source of Fig. 32; locations 412 defining the p-channel devices of Fig. 32; a line 414 providing the control voltage "V control" of Fig. 32; and 915 MHZ option capacitors 416.

Figs. 8.060105AA-DD provide a circuit drawing showing construction details of the divider "txdivider."

Figs. 8.06010501AA-AB provide a circuit drawing showing construction details of a flip-flop "txdivtff" included in the divider.

Figs. 8.0602AA-AB provide a circuit drawing showing construction details of a test mode data selector "txdatasel."

Figs. 8.0603AA-AB provide a circuit drawing showing construction details of a BPSK modulation driver "txbpsk."

#### Details of Frequency Doubler

Analog multipliers are known in the art. An analog multiplier includes two inputs, and includes an output providing a signal that is representative of a multiplication of one of the inputs with the other of the inputs. One known analog multiplier is known as a Gilbert multiplier cell. For a detailed discussion of Gilbert cells, see Four Quadrant Multiplier, B. Gilbert, IEEE Journal of Solid State Circuits,

1 1968, pp. 365-373. Such Gilbert multiplier cells are also described in  
2 detail in Analysis and Design of Analog Integrated Circuits, Paul R.  
3 Gray and Robert G. Meyer, Third Edition, 1993, John Wiley & Sons,  
4 Inc., pp. 667--681. Such Gilbert multiplier cells include two cross-  
5 coupled, emitter-coupled pairs of bipolar junction transistors in series  
6 with an emitter coupled pair of bipolar junction transistors. A Gilbert  
7 multiplier cell employing bipolar junction transistors produces an output  
8 that is the hyperbolic tangent of two input voltages. This is because  
9 a characteristic of bipolar junction transistors is exponential non-linearity.  
10 If the input voltages are sufficiently low, the hyperbolic tangent function  
11 can be approximated as linear, and the circuit behaves as a multiplier  
12 which multiplies together the two input voltages.

13 <sup>sub</sup>  $\Delta$  The multiplier cell originally developed by Gilbert employed  
14 bipolar junction transistors. It is also known to employ MOS transistors  
15 to produce a Gilbert multiplier cell. See, for example, Analog  
16 Integrated Circuits for Communication Principles, Simulation and Design,  
17 Donald O. Pederson and Kartikeya Mayaram, Kuwer Academic  
18 Publishers, Third Printing, 1994, pp. 431-433.

19 Fig. 34 illustrates a frequency doubler circuit 119 that includes a  
20 Gilbert cell 120. The Gilbert cell 120 includes a pair 122 defined by  
21 transistors 124 and 126. The Gilbert cell 120 further includes a pair  
22 128 defined by transistors 130 and 132. The transistors 124 and 126  
23 have sources that are connected together. Thus, the pair 122 is a  
24

1 source coupled pair. The transistors 130 and 132 have sources that are  
2 connected together. Thus, the pair 128 is a source coupled pair.

3 The transistors 126 and 130 have gates that are connected  
4 together to define a first input node. The transistors 124 and 132 have  
5 gates that are connected together to define a second input node. The  
6 transistors 124 and 130 have drains that are connected together, and the  
7 transistors 126 and 132 have drains that are connected together (shown  
8 as a criss-cross pattern in Fig. 34).

9 The Gilbert cell 120 further includes another pair 134 including  
10 transistors 136 and 138 having sources coupled together. Thus, the  
11 pair 134 is a source coupled pair. The pair 134 is in series with the  
12 pairs 122 and 128. More particularly, the transistor 136 has a drain  
13 connected to the sources of the transistors 124 and 126, and the  
14 transistor 138 has a drain connected to the sources of the transistors  
15 130 and 132. The transistor 138 has a gate defining a third input  
16 node, and the transistor 136 has a gate defining a fourth input node.

17 The Gilbert cell 120 further includes an ideal current source 140  
18 driving current from the sources of the transistors 136 and 138 to  
19 ground. The frequency doubler 119 further includes a resistor 142  
20 connected between the drain of the transistor 124 and a voltage, and  
21 a resistor 144 connected between the drain of the transistor 132 and  
22 the voltage. The resistors 142 and 144 define loads for current steering  
23 that produces output voltage swings.  
24

1 For low amplitude signals, the Gilbert cell 120 provides an output  
2 between the drain of the transistor 124 and the drain of the transistor  
3 132 that is an analog multiplication of a first input signal applied  
4 between the first and second input nodes, by a second input signal  
5 applied between the third and fourth input nodes.

6 It is known to use a Gilbert cell to multiply together sine waves  
7 of different phases to produce a doubled frequency (Figs. 34 and 35).  
8 This is based on a known trigonometric relationship:

$$\sin 2\theta = 2 \sin \theta \cos \theta$$

9  
10 Signals that are 180° apart are applied to the first and second input  
11 nodes, and a phase shifter produces 90° shifted signals that are applied  
12 to the third and fourth input nodes. However, in such embodiments,  
13 an integrator is required, and the phase shifter is required to be  
14 feedback controlled, because slight errors in the required 90° phase shift  
15 would otherwise cause the output signals to have different average  
16 values and different amplitudes as shown in Fig. 33. Fig. 33 is a  
17 waveform diagram illustrating the effect of errors in frequency doubler  
18 circuits that necessitates correction, such as by using an integrator and  
19 feedback. Fig. 34 is a circuit schematic illustrating a frequency doubler  
20 circuit that employs an integrator and feedback to solve the problem  
21 illustrated in Fig. 33. Fig. 35 is a waveform diagram illustrating input  
22 and output waves created and employed by a frequency doubler circuit  
23 such as the one shown in Fig. 34.  
24



1 It is desirable to avoid the need for feedback. Frequency  
2 multiplier circuits employing feedback are susceptible to being disturbed.  
3 For example, if substrate noise or an adjacent line switches and causes  
4 a shift at the integrator, the output will be distorted from the desired  
5 output until the integrator has a chance to recover. The integrator can  
6 take a long time to recover. Therefore, it is desirable to eliminate  
7 feedback loops from a frequency multiplier.

8 Fig. 36 is a circuit schematic illustrating a symmetric frequency  
9 doubler circuit 146 that does not require an integrator and feedback to  
10 solve the problem illustrated in Fig. 33. The frequency doubler circuit  
11 of Fig. 36 creates and employs waveforms such as those shown in  
12 Fig. 35.

13 The frequency doubler circuit 146 includes a first Gilbert cell 148,  
14 and a second Gilbert cell 150 coupled to the first Gilbert cell 148.

15 The first Gilbert cell 148 includes a pair 152 defined by  
16 transistors 154 and 156. The transistors 154 and 156 have sources that  
17 are connected together. Thus, the pair 152 is a source coupled pair.  
18 The Gilbert cell 148 further includes a pair 158 defined by transistors  
19 160 and 162. The transistors 160 and 162 have sources that are  
20 connected together. Thus, the pair 158 is a source coupled pair.

21 The transistors 156 and 160 have gates that are connected  
22 together to define a first input node 163. The transistors 154 and 162  
23 have gates that are connected together to define a second input node  
24 165. The transistors 154 and 160 have drains that are connected

1 together, and the transistors 156 and 162 have drains that are connected  
2 together (shown as a criss-cross pattern in Fig. 36).

3 The Gilbert cell 148 further includes another pair 164 including  
4 transistors 166 and 168 having sources coupled together. Thus, the  
5 pair 164 is a source coupled pair. The pair 164 is in series with the  
6 pairs 152 and 158. More particularly, the transistor 166 has a drain  
7 connected to the sources of the transistors 154 and 156, and the  
8 transistor 168 has a drain connected to the sources of the  
9 transistors 160 and 162. The transistor 168 has a gate defining a third  
10 input node 169, and the transistor 166 has a gate defining a fourth  
11 input node 171.

12 The Gilbert cell 148 further includes an ideal current source 170  
13 driving current from the sources of the transistors 166 and 168 to  
14 ground. The frequency doubler 146 further includes a resistor 172  
15 connected between the drain of the transistor 154 and a voltage, and  
16 a resistor 174 connected between the drain of the transistor 162 and  
17 the voltage. The resistors 172 and 174 define loads for current steering  
18 that produces output voltage swings.

19 The second Gilbert cell 150 includes a pair 182 defined by  
20 transistors 184 and 186. The transistors 184 and 186 have sources that  
21 are connected together. Thus, the pair 182 is a source coupled pair.  
22 The Gilbert cell 150 further includes a pair 188 defined by transistors  
23 190 and 192. The transistors 190 and 192 have sources that are  
24 connected together. Thus, the pair 188 is a source coupled pair.

The transistors 186 and 190 have gates that are connected together to define a first input node 193 of the second Gilbert cell 150. The transistors 184 and 192 have gates that are connected together to define a second input node 195 of the second Gilbert cell 150. The transistors 184 and 190 have drains that are connected together, and the transistors 186 and 192 have drains that are connected together (shown as a criss-cross pattern in Fig. 36).

The Gilbert cell 150 further includes another pair 194 including transistors 196 and 198 having sources coupled together. Thus, the pair 194 is a source coupled pair. The pair 194 is in series with the pairs 182 and 188. More particularly, the transistor 196 has a drain connected to the sources of the transistors 184 and 186, and the transistor 198 has a drain connected to the sources of the transistors 190 and 192. The transistor 198 has a gate defining a third input node 199, and the transistor 196 has a gate defining a fourth input node 201.

The Gilbert cell 150 further includes an ideal current source 200 driving current from the sources of the transistors 196 and 198 to ground.

The outputs of the second Gilbert cell are connected to the outputs of the first Gilbert cell. More particularly, the drain of the transistor 184 is connected to the drain of the transistor 154 and the drain of the transistor 192 is connected to the drain of the transistor 162.

1       The first input node 193 of the second Gilbert cell 150 is  
2 connected to the fourth input node 171 of the first Gilbert cell 148.  
3       The third input node 199 of the second Gilbert cell 150 is connected  
4 to the second input node 165 of the first Gilbert cell 148. The fourth  
5 input node 201 of the second Gilbert cell 150 is connected to the first  
6 input node 163 of the first Gilbert cell 148.

7       In operation, a first sinusoidal signal is applied to the second  
8 input node 165 of the first Gilbert cell 148. A second sinusoidal  
9 signal,  $180^\circ$  out of phase with the first sinusoidal signal, is applied to  
10 the first input node 163 of the first Gilbert cell 148 (and to the fourth  
11 input node of the second Gilbert cell 150). A third sinusoidal signal,  
12  $90^\circ$  out of phase with the first sinusoidal signal, is applied to the  
13 second input node 195 of the second Gilbert cell 150. A fourth  
14 sinusoidal signal,  $270^\circ$  out of phase with the first sinusoidal signal, is  
15 applied to the first input node of the second Gilbert cell 150. This  
16 relationship of phases on the inputs to the first and second Gilbert  
17 cells causes the output to be symmetrical so that the problem of  
18 Fig. 33 is avoided without the need for feedback. Even with slight  
19 errors in phases between the input signals, a symmetrical output is  
20 produced.

21       Generally speaking, each Gilbert cell adds current from bottom  
22 transistors to top transistors through the resistor loads to form output  
23 voltages. In the illustrated embodiment, a phase arrangement applied  
24

1 to the upper Gilbert cell is generally reversed for the bottom Gilbert  
2 cell so undesirable offsets cancel each other.

3 In one embodiment, the second, third, and fourth input sinusoidal  
4 signals are derived from the first input sinusoidal signal using a simple  
5 four stage differential oscillator.

6 A doubled frequency is thus obtained at the outputs, which are  
7 defined at the drain of the transistor 154 and the drain of the  
8 transistor 162, without the need for an integrator and feedback.

9 Figs. 8.0604AA-AB provide a circuit drawing of the frequency  
10 doubler "txdoubler." The frequency doubler circuit "txdoubler" includes  
11 a doubler core "txfdbl" having two tiers of transistors. The two tiers  
12 of transistors are shown in Figs. 8.060401AA-FE as being a top tier and  
13 a bottom tier. The frequency doubler requires different levels  
14 depending on whether the top tier of transistors or bottom tier of  
15 transistors are driven by a particular phase. The frequency doubler  
16 "txdoubler" therefore includes driver amplifiers "txfdbldrv" which provide  
17 that level shifting. There is no intended phase shift introduced by the  
18 driver amplifiers.

19 Figs. 8.060401AA-FE provide a circuit drawing of the frequency  
20 doubler core "txfdbl." The frequency doubler core "txfdbl" includes  
21 level shifting circuitry. The level shift is a little level shift, and is  
22 accomplished by a resistor and capacitor shown at the top of the right  
23 stack (Fig. 8.060401AD). The level shift is performed in order to  
24

1 adjust output levels down in voltage because this frequency doubler core  
2 drives another frequency doubler.

3 Figs. 8.0605AA-AB provide a circuit drawing of the frequency  
4 doubler "txdoubler2." The frequency doubler "txdoubler2" is substantially  
5 similar to the first frequency doubler "txdoubler." The main difference  
6 has to do with the bias arrangements for the driver amps and for the  
7 doubler core. In an alternative embodiment, the first and second  
8 frequency doublers "txdoubler" and "txdoubler2" are identical.

9 Figs. 8.060501AA-CD provide a circuit drawing showing  
10 construction details of the doubler driver amplifier "txfdbldrv."

11 Figs. 8.060502AA-CD provide a circuit drawing showing  
12 construction details of a second doubler driver amplifier "txfdbldrv2"  
13 included in the frequency doubler "txdoubler2." The second doubler  
14 driver amplifier "txfdbldrv2" include a bias diode. The doubler driver  
15 amplifier "txfdbldrv2" includes circuitry (the criss-cross configuration in  
16 Figs. 8.060502AA-CD) where bi-phase (binary phase shift keying)  
17 modulation is performed. This is where a phase can be switched from  
18 one side to another by the state of two inputs "BPMODINP" and  
19 "PMODINN." Thus, a phase reversal can be accomplished in this  
20 circuit.

21 Figs. 8.060503AA-FE provide a circuit drawing of a frequency  
22 doubler core "txfdbl2." The frequency doubler core "txfdbl2" is  
23 substantially identical to the frequency doubler core "txfdbl" except for  
24 the biasing transistors.

## Details of Single Antenna Receiver and Active Transmitter

Fig. 50 provides a simplified circuit schematic showing the antenna 44 being shared by the active transmitter and the Schottky diode detector 84. The Schottky diode detector 84 was described above in detail in connection with Fig. 29, like reference numerals indicating like components.

The detector 84 includes a Schottky diode 86 having an anode connected to the antenna 44 and having a cathode. The detector 84 further includes an ideal current source 88 connected to the cathode of the Schottky diode 86 and driving current through the antenna and Schottky diode 86 in the direction from the anode to the cathode. The detector 84 further includes a capacitor 90 connected between the cathode of the Schottky diode 86 and ground and providing a radio frequency short to ground. The detector 84 further includes a capacitor 92 having a first terminal connected to the cathode, having a second terminal defining an output of the detector 84, providing an AC short to video frequency, and defining the output of the detector 84.

The active transmitter is described elsewhere herein, and is illustrated as a block 330 in Fig. 50.

The antenna is a loop antenna and has one end connected to a bias voltage ( $V_{dd}$ ) and has another end connected to the anode of the Schottky diode 86.

1 The transmitter has an antenna output (or RF output) 332, and  
2 the detector 84 has an antenna input (or RF input) 334. In the  
3 illustrated embodiment, the integrated circuit 16 having the  
4 transmitter 330 and detector 84 includes a contact connected to the  
5 antenna output 332 and accessible from outside the IC package; and a  
6 contact connected to the antenna input 334 and accessible from outside  
7 the IC package. These contacts are connected together by a short  
8 outside the package. This provides for flexibility in that different  
9 antenna configurations are possible, separate antennas can be used for  
10 the detector 84 and transmitter 330, if desired, an external amplifier can  
11 be used to amplify the output of the transmitter 330, etc.

12 The detector and transmitter do not operate simultaneously.

13 In one embodiment, the integrated circuit 16 further includes a  
14 pull up transistor 336 connected to the cathode of the Schottky diode  
15 86 and configured to connect the cathode to the bias voltage (Vdd)  
16 when the transmitter is operating. The pull up transistor 336 can be  
17 included if necessary so the detector does not interfere with the  
18 transmitter 330 while the transmitter 330 is transmitting.

19 By using a common antenna for the active transmitter and the  
20 Schottky diode detector, space savings are achieved.

21 The active transmitter 330 is shown in greater detail in Fig. 51.  
22 The active transmitter includes a differential pair 338 of transistors  
23 driven by the frequency doubler. The function of the differential pair  
24 338 is to steer current to the antenna 44 or away from the antenna



1 44. If bi-phase modulation is employed, the differential pair 338 steers  
2 one phase or the other phase to the antenna 44. More particularly,  
3 if bi-phase modulation is employed, then a signal on line "ENABLEAM"  
4 (see Figs 8.06AA-ED, and 8.0605AA-AB to 8.0608AA-BB) is low and  
5 the leftmost of three current steering transistors (sources connected to  
6 the current source) is off because its gate is low. Current is then  
7 steered to the antenna by the transistor shown on the right. Its phase  
8 is determined in an earlier stage. The other phase is present in the  
9 middle transistor. When data is reversed the current phases switch  
10 sides in response to the earlier stage. If amplitude modulation is  
11 employed, the differential pair either sends current to the antenna 44,  
12 or is sends none to provide on/off keying. More particularly, in the  
13 amplitude modulation mode, a signal on line "ENABLEAM" is high and  
14 current is steered to the antenna by the transistor shown to the right  
15 if a signal on line "AMDATA" is high, and the current is steered to  
16 Vdd (not to the antenna) if the signal on line "AMDATA" is low.

17 Figs. 8.0606AA-IE provide a circuit drawing of a transmitter power  
18 amplifier "txpoweramp." The transmitter power amplifier includes a  
19 frequency doubler, shown in the left half of Figs. 8.0606AA-IE. In the  
20 illustrated embodiment, the frequency doubler receives inputs at 1.22  
21 GHz, and provides outputs at 2.44 GHz. The transmitter power  
22 amplifier includes the differential pair of transistors, shown on the right  
23 side of Figs. 8.0606AA-IE, driven by the frequency doubler. The  
24 differential pair steers current to the antenna or away from the

1 antenna, as described above. If bi-phase modulation is employed, the  
2 differential pair steers one phase or the other phase to the antenna.  
3 If amplitude modulation is employed, the differential pair either sends  
4 current to the antenna, or it sends none to provide on/off keying.

5 Figs. 8.0607AA-JJ provide a circuit drawing of a transmitter bias  
6 generator "txbias." The transmitter bias generator includes various  
7 current mirrors in order to provide the proper bias currents to the  
8 various blocks of the transmitter "tx."

#### 9 10 Details of Single Antenna Receiver and Backscatter Transmitter

11 Fig. 52 provides a simplified circuit schematic showing an antenna  
12 350 being shared by the backscatter transmitter and the Schottky diode  
13 detector 84, in a manner similar to the antenna sharing possibility  
14 described in connection with Figs. 50-51. The Schottky diode detector  
15 84 was described above in detail in connection with Fig. 29, like  
16 reference numerals indicating like components.

17 In the illustrated embodiment, the antenna 350 is a loop antenna  
18 and has one end connected to a bias voltage (Vdd) and has another  
19 end connected to the detector 84 via a detector input illustrated as  
20 RXANT in Fig. 52. For antenna sharing with a backscatter transmitter,  
21 capacitors 352 and 354 external of the integrated circuit 16 are  
22 employed, as illustrated in Fig. 52, to isolate the antenna from the  
23 backscatter antenna driver when the detector is using the antenna.

24 The detector and transmitter do not operate simultaneously.

1 By using a common antenna for the backscatter transmitter and  
2 the Schottky diode detector, space savings are achieved.

3 In an alternative embodiment shown in Fig. 53, a single  
4 antenna 350 is shared by the detector 94 (shown in Fig. 30 and  
5 described elsewhere herein) and a backscatter transmitter. An n-channel  
6 transistor 356 is provided having power electrodes connected to opposite  
7 ends of the antenna, and having a control electrode connecting to  
8 transmitter modulation circuitry. The control electrode is held low when  
9 the antenna is being used by the receiver.

10 Figs. 8.0608AA-BB provide a circuit drawing of a modulated  
11 backscatter transmitter "txmbs." The modulated backscatter transmitter  
12 "txmbs" includes circuitry that creates non-overlapping drive signals. The  
13 modulated backscatter transmitter "txmbs" includes primary antenna ports  
14 "BS1" and "BS2." Each of these antenna ports is intended to be  
15 connected to one-half of a dipole antenna having a length appropriate  
16 for the transmission frequency. In the illustrated embodiment, the  
17 halves of the dipole antenna have respective sizes appropriate for 2.44  
18 Ghz. The halves of the dipole antenna are not included on the  
19 integrated circuit 16, in the illustrated embodiment, but are instead  
20 provided "off chip." Other antenna arrangements are possible.

21 The modulated backscatter transmitter "txmbs" further includes an  
22 n-channel transistor marked 900 micron in Figs. 8.0608AA-BB, and two  
23 n-channel pull-up transistors marked 100 micron and respectively  
24 connected between a voltage vdd! and the 900 micron transistor. When

1 the gate of the transistor marked 900 micron is high, then the two  
2 dipole halves are shorted together with a fairly low impedance (e.g., on  
3 the order of 15 Ohms, plus any bond wire impedance that might be  
4 present depending on how the device is packaged). The antenna  
5 becomes substantially similar to a single half-wavelength antenna. In a  
6 backscatter mode, when the two halves of the antenna are shorted  
7 together, the antenna reflects a portion of the power being transmitted  
8 by the interrogator. In the other state, the gate of the 900 micron  
9 transistor is low. The 900 micron transistor is then off, but the two  
10 100 micron transistors that pull up the voltage vdd! are on, lifting  
11 antenna ports "BS1" and "BS2" both up to a voltage of vdd! minus an  
12 n-channel  $V_t$ . The two antenna ports "BS1" and "BS2" are then  
13 isolated from each other by an open circuit. This isolation changes the  
14 radar cross-section of the dipole antenna dramatically from when the  
15 two halves are shorted together. The antenna becomes substantially  
16 similar to two quarter wavelength antennas. In a Backscatter mode,  
17 when the two halves of the antenna are isolated, the antenna reflects  
18 very little of the power transmitted by the interrogator.

19 The modulated backscatter transmitter "txmbs" further includes  
20 cross-coupled circuitry shown near the middle in Figs. 8.0608AA-BB.  
21 The cross-coupled circuitry is provided to make sure that both the pull  
22 up transistors and the shorting device are not on at the same time.

23 The modulated backscatter transmitter "txmbs" further includes  
24 another antenna port "BS3" that is intended to be used when the

1 integrated circuit 16 is packaged in the standard SOIC package. The  
2 antenna port "BS3" provides another option for configuring a backscatter  
3 antenna. The antenna port "BS3" supplies a one milliamp current and  
4 can drive an external PIN diode that would be situated between the  
5 two halves of the dipole antenna or any other suitable antenna. The  
6 other side of that external PIN diode can be returned to either the  
7 antenna port "BS1" or "BS2." Because PIN diodes are good shorting  
8 and opening devices for backscatter applications, the transmission range  
9 of a device 12 built with the integrated circuit 16 can be extended over  
10 the range that is obtained using only the internal circuitry of the  
11 integrated circuit 16. This is at the expense of the need for an  
12 external component and an accompanying increase in cost of the device  
13 12.

14 Figs. 8.07AA-BB provide a partial circuit drawing illustrating a 915  
15 MHZ transmitter "tx915" that can be included instead of the active  
16 transmitter described above. The transmitter "tx915" has one less stage  
17 of doubling. The chip rate also changes.

18 Figs. 8.0701AA-CB provide a circuit drawing of a VCO stage  
19 modified for use with the 915 MHZ transmitter "tx915" by adding  
20 capacitors to the output. The modified VCO stage is manufactured by  
21 making a metal mask adjustment employed in an alternative embodiment  
22 of the invention.

23 Figs. 9AA-CB provide a circuit drawing of the analog processor  
24 "analgproc." The analog processor "analgproc" includes a master bias

1 source "mbs," voltage regulators "vrg" and "vrgtx," a bias OK circuit  
2 "biasok," an analog port current source "aportcs," an analog multiplexor  
3 decoder "asl," a random number clock generator "rcg" for the pseudo  
4 random number generator, a power up detector "pup," and an analog  
5 to digital (A/D) converter "ada\_new." The analog multiplexor decoder  
6 "asl" is an address selector used, in one embodiment, to choose from  
7 among various possible inputs to the analog to digital converter. The  
8 power up detector "pup" puts out a master reset pulse upon power up.  
9 The power up detector also puts out another pulse that lasts throughout  
10 a power up cycle in which the processor performs operations  
11 appropriate upon power up, the last operation being to reset the wake  
12 up pulse. The random number clock generator "rcg" generates random  
13 numbers for use in arbitration schemes and generates a pseudo-random  
14 sequence. The master bias source "mbs" includes a band gap regulator.  
15 The voltage regulators "vrg" and "vrgtx" generate supply voltages for  
16 various blocks of circuitry. The bias OK circuit "biasok" determines  
17 when the regulator voltage has reached a final level, and then enables  
18 the circuitry that is driven by the regulator.

#### 20 Details of Low Battery Detection

21 The integrated circuit 16 includes a differential I/O op-amp or  
22 comparator comparing the voltage of the battery with a predetermined  
23 voltage (e.g., with band gap voltage). A low battery signal is generated  
24 if the voltage of the battery is less than the predetermined voltage.

1 More particularly, one of the status registers is a battery status register  
2 and has a value indicating if the voltage of the battery is less than the  
3 predetermined voltage. The transmitter "tx" transmits the value of this  
4 battery status register via radio frequency when responding to commands  
5 from the interrogator. In the illustrated embodiment, a battery voltage  
6 detector is shown in Figs. 16 (and in Figs 11 and 9.010304AA-BB);  
7 however, the battery voltage detector can be provided in a different  
8 location of the integrated circuit 16.

9 Figs. 9.01AA-DH provide a circuit drawing of the analog to digital  
10 converter "ada\_new." In the illustrated embodiment, the analog to  
11 digital converter is substantially disabled and is used only to provide a  
12 latch circuit for reading the low battery voltage detector. In a  
13 preferred embodiment, the analog to digital converter is used in  
14 connection with analog sensors and to provide alarm signals when  
15 thresholds are exceeded.

16 Figs. 9.0101AA-CK provide a circuit drawing showing construction  
17 details of the differential I/O op-amp "dopamp" included in the analog  
18 to digital converter.

19 Figs. 9.0102AA-DH provide a circuit drawing showing construction  
20 details of an analog divider (divide by two) "adaprescale" included in  
21 the analog to digital converter.

22 Figs. 9.0103AJ-FP provide a circuit drawing showing construction  
23 details of a control PLA "adactl\_new" included in the analog to digital  
24 converter circuit of Figs. 9.01AA-DH.

1 Figs. 9.010301AA-CC provide a circuit drawing showing construction  
2 details of a clock generator "adacgen\_new" included in the control PLA.

3 Figs. 9.010302AA-AB provide a circuit drawing showing construction  
4 details of a control output driver "adacdrv\_new" included in the control  
5 PLA.

6 Figs. 9.010303AA-AB provide a circuit drawing showing construction  
7 details of a control output driver "adacdrvn\_new" included in the control  
8 PLA.

9 Figs. 9.010304AA-BB provide a circuit drawing showing construction  
10 details of a data latch "adadlat\_new" which is included in the control  
11 PLA and which is presently used as part of the battery voltage  
12 detector.

13 Figs. 9.0104AA-DD provide a circuit drawing showing construction  
14 details of the analog bias circuit "adabias\_new" included in the analog  
15 to digital converter.

16 Figs. 9.02AA-DK provide a circuit drawing of a Vdd power up  
17 detector "pup" included in the analog processor. The power up  
18 detector puts out a master reset pulse upon power up. The power up  
19 detector also puts out another pulse that extends throughout a power  
20 up cycle while the processor performs a number of operation, the last  
21 one of which is to reset the wake up pulse. The power up detector  
22 uses a thermal voltage generator, which is a circuit such as is used for  
23 the low power current controlled oscillator, described above. The  
24 thermal voltage generator generates a small current. The power up



1 circuit "pup" further includes current mirrors, and a capacitor illustrated  
2 near the top center of Figs. 9.02AA-DK. The current mirrors mirror  
3 the small current generated by the thermal voltage generator. The  
4 mirrored current holds down one side of the capacitor illustrated near  
5 the top center of Figs. 9.02AA-DK. When the power supply first rises  
6 from zero to its final value, whatever that might be (e.g., 3 Volts or  
7 5 Volts), the capacitor couples up the bottom plate causing a signal to  
8 rise on a line "PWRUP." The small mirrored current then slowly  
9 discharges the bottom plate until "PWRUP" switches back low. A  
10 signal from before the final inverter producing "PWRUP" goes down to  
11 circuitry shown on the lower right of Figs. 9.02AA-DK. That circuitry  
12 provides a hard pull down on the bottom of the capacitor to impede  
13 any switching back and forth. After the "PWRUP" pulse, the circuitry  
14 switches the bottom of the capacitor back down to ground much more  
15 rapidly than the small mirrored currents could. The circuitry then  
16 resets so that the only thing left holding the bottom of the capacitor  
17 low is the small current mirrored from the thermal voltage generator.  
18 The power up detector also generates another pulse on a line  
19 "WAKEUP" shown on the right of Figs. 9.02AA-DK. This pulse goes  
20 high at the same time as the pulse on line "PWRUP" but does not  
21 come down at the same time. Instead, the pulse on the line  
22 "WAKEUP" does not come down until the processor issues a wake up  
23 acknowledge signal on line "WUACK." The processor does not issue  
24

1 the wake up acknowledge signal until completion of running of a wake  
2 up program stored in the ROM.

3 Figs. 9.03AA-BB provide a circuit drawing of a master bias source  
4 "mbs" included in the analog processor. The master bias source "mbs"  
5 includes a band gap reference generator "mbs\_bgr" to generate bias  
6 voltages for various circuits of the integrated circuit 16. The master  
7 bias generator includes a temperature compensated current generator  
8 "mbs\_cur" that is employed in one embodiment of the invention, but is  
9 disconnected in the illustrated embodiment. The master bias source  
10 further includes a reference current generator "mbs\_iref" that comprises  
11 current mirrors to replicate a reference current (e.g., 2.5 microAmps).

12 Figs. 9.0301AA-DJ provide a circuit drawing showing construction  
13 details of a band gap reference generator "mbs\_bgr" included in the  
14 master bias source. Band gap reference generators produce a reference  
15 voltage, and are known in the art. See, for example, Analysis and  
16 Design of Analog Integrated Circuits, Paul R. Gray and Robert G.  
17 Meyer, John Wiley & Sons. The reference voltage produced is  
18 approximately equal to the band gap voltage of silicon, which is  
19 approximately 1.2 Volts. A band gap reference generator generates a  
20 voltage output that is independent of power supply and temperature.

21 Figs. 9.0302AA-DI provide a circuit drawing showing construction  
22 details of a temperature compensated current generator "mbs\_cur"  
23 included in the master bias source.  
24

1 Figs. 9.0303AA-CF provide a circuit drawing of the reference  
2 current generator "mbs\_iref" included in the master bias source. The  
3 reference current generator "mbs\_iref" biases various circuits of the  
4 integrated circuit 16. The reference current generator "mbs\_iref"  
5 includes current mirrors that replicate incoming current so that the  
6 reference current generator can supply the same value current to a  
7 number of different circuit blocks.

8 Figs. 9.04AA-CE provide a circuit drawing of the voltage regulator  
9 "vrg" included in the analog processor. The voltage regulator includes  
10 an op-amp having an input receiving a reference voltage "VREF" (which  
11 is approximately 1.2 Volts). The voltage regulator further includes a  
12 large p-channel device driven by the output of the op-amp. In the  
13 illustrated embodiment, the p-channel device is made up of a plurality  
14 of p-channel devices connected together in parallel. The voltage  
15 regulator further includes an output node "VREG" driven by the  
16 plurality of p-channel devices. The voltage regulator further includes  
17 a resistor divider, shown along the middle of the right side of Figs.  
18 9.04AA-CE, connected to the output "VREG." The resistor divider  
19 includes a fifty percent point (having a voltage of half of the voltage  
20 at the output node "VREG") that is fed back to another input of the  
21 op-amp so that the voltage at the output node "VREG" is required to  
22 be two times the input voltage "VREF" to complete the feedback. In  
23 the illustrated embodiment, a number of individual regulators are  
24 employed in order to isolate power supplies to different areas of the

1 circuit. However, in alternative embodiments, a reduced number of  
2 voltage regulators are employed.

3 Figs. 9.05AA-FE provide a circuit drawing of the voltage regulator  
4 "vrgtx" included in the analog processor. The voltage regulators "vrg"  
5 and "vrgtx" generate supply voltages approximately equal to two times  
6 band gap voltage (about 2.4 Volts) for various blocks of circuitry. The  
7 voltage regulator "vrgtx" provides substantially the same output voltage  
8 as the voltage regulator "vrg"; however, it has a bigger drive capability.  
9 The voltage regulator "vrgtx" is connected to the active transmitter  
10 which requires a lot of current.

11 Figs. 9.0501AA-CD provide a circuit drawing showing construction  
12 details of an operational amplifier without compensation "opampnc"  
13 included in the voltage regulator.

14 Figs. 9.06AA-DD provide a circuit drawing of a bias OK detector  
15 "biasok" included in the analog processor. The bias OK detector puts  
16 out a signal indicating that regulator voltage going to the receiver is at  
17 or near full level. The bias OK detector includes a voltage detector.  
18 A delay is built in so that adequate time is allowed. The bias OK  
19 detector allows biases to stabilize before releasing the clock recovery  
20 circuit and the wake up test logic.

21 Figs. 9.07AA-EG provide a circuit drawing showing construction  
22 details of an analog port current source "aportcs" included in the analog  
23 processor. The analog port current source "aportcs" provides a current  
24 which can be used to bias sensors external to the integrated circuit 16.

1 The value of the current supplied by the analog port current source  
2 "aportcs" is selected from several available values by a radio frequency  
3 command. In the illustrated embodiment, the analog port is not  
4 employed. However, in alternative embodiments, an analog port is used.

5 Figs. 9.08AA-CC provide a circuit drawing showing construction  
6 details of an analog multiplexer decoder "asl" included in the analog  
7 processor. The analog multiplexer decoder "asl" is an address selector.  
8 More particularly, in a preferred embodiment, the analog multiplexer  
9 decoder "asl" is used to choose from among various possible analog  
10 inputs to the analog to digital converter.

11 The random number clock generator "rcg" for the pseudo random  
12 number generator is shown in greater detail in Figs. 9.09AA-BB. The  
13 random clock generator generates random numbers for use in the  
14 arbitration scheme of the protocol to sort between multiple responding  
15 devices 12.

#### 16 17 Details of Low Power Pseudo Random Number Generator

18 The device includes a random clock generator "rcg" including a  
19 linear feedback shift register "rcg\_osc" that has a plurality of stages and  
20 that generates a pseudo-random sequence. The random clock generator  
21 "rcg" includes an oscillator "rcg\_osc" that supplies clock signals to the  
22 linear feedback shift register. The device includes a low current  
23 generator, such as a thermal voltage generator, to drive the oscillator  
24 that supplies clock signals to the linear feedback shift register. The

1 shift register has two modes of operation; namely, a low power mode,  
2 and a high power mode. The random clock generator includes current  
3 mirrors referenced to the low current generator. In the low power  
4 mode, the current to each stage of the shift register is limited by the  
5 current mirrors. In the high power mode, the current mirror device  
6 gates are driven to full supply voltages. This allows the shift register  
7 to operate at a higher frequency appropriate for shifting the random  
8 number into the processor.

9 This technique is illustrated, with reference to an inverter, in a  
10 simplified schematic in Fig. 37. Fig. 37 shows a circuit including series  
11 connected p-type transistors 210 and 212, and series connected n-type  
12 transistors 214 and 216 which are connected in series with the p-type  
13 transistors 210 and 212. The transistors 210, 212, 214, and 216 are  
14 connected between a positive voltage "V+" and ground. The transistor  
15 210 has a gate connected to a voltage "V BIAS P" and the transistor  
16 216 has a gate connected to a voltage "V BIAS N."

17 When "V BIAS N" and "V BIAS P" are controlled by a low  
18 current current mirror (low power mode), the turn-on voltages of  
19 transistors 210 and 216 are small and current through inverter  
20 transistors 212 and 214 is limited. When "V BIAS N" is pulled to  
21 "V+" and "V BIAS P" is pulled to ground, the inverter operates at  
22 full speed.

23 Figs. 9.09AA-BB provide a circuit drawing showing construction  
24 details of the random clock generator "rcg" included in the analog

1 processor. The random clock generator "rcg" includes a low power  
2 oscillator and bias generator "rcg\_osc." The random clock generator  
3 "rcg" further includes the linear feedback shift register "rcg\_sreg." The  
4 random clock generator "rcg" further includes a clock generator  
5 "rcg\_clkgen" which generates non-overlapping versions of the clock which  
6 drives the linear feedback shift register "rcg\_osc." The linear feedback  
7 shift register "rcg\_osc" generates the pseudo-random sequence. The  
8 random clock generator further includes circuitry (shown below the linear  
9 feedback shift register in Figs. 9.09AA-BB) for switching between clock  
10 schemes. This circuitry includes an n-channel device and a p-channel  
11 device (shown as circles with x's through them in Figs. 9.09AA-BB)  
12 allowing connection or blocking connection between the input and the  
13 output of the devices. The alternate clock sources are state one "S1,"  
14 state three "S3," and phase two "P2" from the processor clock. The  
15 shift register is operable in a high power mode and in a very low  
16 power mode. When the processor wants a random number from the  
17 shift register "rcg\_osc," these clocks are used and the shift register is  
18 operated in the high power mode to shift eight bits at a time in serial  
19 fashion into the processor. A total of sixteen bits are transferred, so  
20 two transfers of eight bits each take place. At other times, the shift  
21 register is in the very low power mode and is driven by the clock  
22 generated by the low power oscillator. In this manner, the shift  
23 register "rcg\_osc" sequences through its pseudo-random sequence  
24

continuously in the background until the shift register is called upon to provide a number.

Figs. 9.0901AA-CH provide a circuit drawing showing construction details of the linear feedback shift register "rcg\_sreg" included in the random clock generator. In the illustrated embodiment, the linear feedback shift register "rcg\_sreg" is a [17,3] shift register having an output in register seventeen. The input to the first register is the exclusive-or of registers seventeen and three. The linear feedback shift register "rcg\_sreg" includes seventeen stages, so it produces a sequence of  $2^{17}-1$ . Therefore, the odds of two devices 12 being at the same place in the sequence are low.

Figs. 9.090101AA-CC provide a circuit drawing showing construction details of a shift register zero bit "rcg\_sregbit0" included in the linear feedback shift register. This bit is different from others so that it can power up in a particular state. The shift register will function to deliver a sequence of pseudo-random numbers as long as all registers are not allowed to go to zero. Therefore, the zero bit "rcg\_sregbit0" of the shift register is altered to guarantee that it will be a one on power up. The shift register bit "rcg\_sregbit0" shown in Figs. 9.090101AA-CC also includes a series of n-channel and p-channel devices to limit current in the logic gates. When the random clock generator is in the low power mode, the bias voltages on these series devices allow only very small currents; however, when the random clock generator is operating in the high power mode (when the processor is



1 shifting in a random number) then these nodes are driven to full  
2 supply. A line "BIASN" will be driven to Vdd, and a line "BIASP"  
3 will be driven to ground. Then the logic of the random clock  
4 generator operates in a normal mode.

5 Figs. 9.090102AA-BB provide a circuit drawing showing construction  
6 details of a shift register bit "rcg\_sregbit" included in the linear  
7 feedback shift register.

8 Figs. 9.0902AA-FL provide a circuit drawing showing construction  
9 details of the low power oscillator and bias generator "rcg\_osc" included  
10 in the random clock generator. The low power oscillator includes a  
11 thermal generator, as in previously described circuitry. The low power  
12 oscillator and bias generator "rcg\_osc" further includes bias voltage  
13 generators shown in the middle and at the bottom in Figs. 9.0902AA-  
14 FL. The bias voltage generator shown at the bottom in Figs.  
15 9.0902AA-FL includes extra transistors to allow switching between high  
16 and low power states.

17 Figs. 9.0903AA-CC provide a circuit drawing showing construction  
18 details of a clock generator "rcg\_clkgen" included in the random clock  
19 generator.

20 The PN processor "pnproc" shown in Figs. 6AA-EK is the spread  
21 spectrum processing circuit 40 shown in Fig. 5. The PN processor  
22 "pnproc" performs spread spectrum processing. Spread spectrum  
23 modulation is described elsewhere. The PN processor "pnproc" is shown  
24 in greater detail in Figs. 10AA-DD.

The PN processor "pnproc" shown in Figs. 10AA-DD includes a digital PN correlator "dcorr." The correlator receives a data stream on line "RXCHIPS" that comes from the receiver. The correlator has a thirty-one chip register and performs a comparison of the chip pattern of the incoming data stream with the expected thirty-one chip pattern. When there is a total or near match, the correlator "dcorr" puts out a high signal (a one) on line "RXDATA." When there is a nearly total mismatch, the correlator "dcorr" puts out a low signal (a zero) on line "RXDATA." Every thirty-one chips, "RXDATA" either changes state or does not change state, depending on whether the PN sequence was inverted or not inverted (i.e., depending on whether a zero or one was defined by the thirty-one chip sequence). The output of the correlator "dcorr" on line "RXDATA" is a sequence of true, non-encoded, data bits of ones and zeros.

The PN processor further includes a PN lock detector "pnlockdet." The lock detector is a circuit that determines whether a preamble is present. In the illustrated embodiment, the preamble is all zeros. Therefore, the lock detector "pnlockdet" determines whether or not a certain length of zeros have occurred in a row. In the illustrated embodiment, the lock detector "pnlockdet" determines whether or not four zeros occurred in a row. The lock detector "pnlockdet" has an output that is connected to the serial input output circuit "sio" in the processor, and enables the processor to look for the Barker or start code.

1 The PN processor further includes a clock "pngclk." The clock  
2 "pngclk" is a clock generator that is based on a clock signal  
3 "CHIPCLK" produced by the digital clock and data recovery circuit  
4 "dcr." The clock "pngclk" puts out non-overlapping true and  
5 compliment versions of the clock and these are used to drive circuitry  
6 in the PN processor.

7 The PN processor further includes a shift register "pngshr." The  
8 shift register is a block of logic that can be used to generate a thirty-  
9 one chip sequence, a sixty-three chip sequence, and a two hundred and  
10 fifty-five chip sequence. A thirty-one chip sequence is always used for  
11 receiving, but for transmitting multiple selections are available. In the  
12 illustrated embodiment, the integrated circuit 16 is wired to allow a  
13 selection between thirty-one and sixty-three chips. In alternative  
14 embodiments, it can be wired to allow a selection between thirty-one  
15 and two hundred and fifty-five chips, or between thirty-one and sixty-  
16 three chips. In the receive mode, the PN sequence is not used  
17 explicitly, except that the middle chip and the last chip in the sequence  
18 are detected, and those signals are used by circuitry labelled "Bit Rate  
19 Clock Generator" in Figs. 10AA-DI to generate a bit rate clock for the  
20 transmitter and receiver. Thus, the output of this shift register "pngshr"  
21 is used to generate a bit rate clock, on line "TRCLK." In the  
22 transmit mode, if a modulation scheme has been selected that uses  
23 spread spectrum encoding, the output of this shift register is used to  
24 encode the data.

1 The PN processor further includes a differential and PN encoder  
2 "dpenc." The differential encoder performs differential encoding and PN  
3 encoding. The differential encoder includes an input connected to a  
4 line "TXDATA." The data on line "TXDATA" is differential encoded  
5 by the differential encoder, if differential encoding is selected. Both  
6 polarities of differential encoding are provided for and are selected  
7 depending on the desired modulation scheme. The differential and PN  
8 encoder can also impress the PN code on the data "TXDATA" if this  
9 is selected.

10 The PN processor further includes a PSK/FSK generator "fskgen."  
11 In the illustrated embodiment, PSK (phase shift keying) is performed by  
12 the PSK/FSK generator "fskgen." In an alternative embodiment, FSK  
13 (frequency shift keying) is performed by the PSK/FSK generator  
14 "fskgen." The generator "fskgen" has both a last chip complement  
15 output "FSKLASTCHIP" and a mid chip complement output  
16 "FSKMIDCHIP." These outputs are connected to the bit rate clock  
17 generator and override the outputs from the PN generator shift register  
18 "pngshr". The bit rate clock generator then generates the appropriate  
19 bit rate clock.

20 The PN processor further includes D type flip-flops "pnddff," one  
21 of which is included in the bit rate clock generator.

22 The PN processor further includes circuitry shown on the lower  
23 right in Figs. 10AA-DD that provides for test modes. This circuitry  
24 provides a way to bring a modulating signal for the transmitter out to



1 into the "Iagree" line to overcome the threshold set by the current  
2 biasing in the upper comparator, a one is detected, and the circuit puts  
3 out a digital one. If, on the other hand, the currents in the  
4 "Idisagree" line are high enough to overcome the threshold set by the  
5 current biasing in the lower comparator, a zero is detected, and the  
6 circuit puts out a digital zero. In other cases, the output does not  
7 change. The correlator further includes circuitry shown on the right of  
8 Figs. 10.01AA-DJ that synchronizes the data stream out of the correlator  
9 and into other information processing circuitry.

10 Figs. 10.0101AA-BG provide a circuit drawing showing construction  
11 details of the PN correlator shift register "dcorr\_sreg" included in the  
12 PN correlator. The shift register "dcorr\_sreg" performs a chip by chip  
13 comparison between the incoming data stream and the expected thirty-  
14 one chip PN sequence. For each chip that agrees, the shift register  
15 "dcorr\_sreg" puts out a current on a line "Iagree." For each chip that  
16 is in disagreement, the shift register "dcorr\_sreg" puts out a current on  
17 a line "Idisagree."

18 Fig. 10.010101 provides a circuit drawing showing construction  
19 details of a PN correlator bit "dcorr\_bit" included in the PN correlator  
20 shift register.

21 Fig. 10.01010101 provides a circuit drawing showing construction  
22 details of a shift register cell "dcorr\_sregbit" included in the PN  
23 correlator bit.  
24

1 Figs. 10.0102AA-CN provide a circuit drawing showing construction  
2 details of a correlator bias generator "dcorr\_bias" included in the PN  
3 correlator.

4 Figs. 10.02AA-BE provide a circuit drawing showing construction  
5 details of a PN lock detector "pnlockdet" included in the PN processor.  
6 The PN lock detector "pnlockdet" detects the preamble by counting.  
7 For example, in the illustrated embodiment, the PN lock detector  
8 "pnlockdet" determines that a preamble has been received if the lock  
9 detector counts four consecutive zeros in a row. If the PN lock  
10 detector does not achieve the four consecutive zeros, it resets and starts  
11 counting again.

12 Figs. 10.0201AA-AB provide a circuit drawing showing construction  
13 details of a counter bit "lockcounterbit" included in the PN lock  
14 detector.

15 Figs. 10.03AA-AB provide a circuit drawing showing construction  
16 details of the PN generator clock "pngclk" included in the PN processor.  
17 The PN generator clock is a non-overlapping clock generator.

18 Figs. 10.04AA-CE provide a circuit drawing showing construction  
19 details of a PN generator shift register "pngshr" included in the PN  
20 processor. The PN generator shift register has select lines so that  
21 various sized PN sequences can be generated (e.g. thirty-one, sixty-three,  
22 or two hundred and fifty-five chip sequences). The PN generator shift  
23 register also includes circuitry for generating mid chip and last chip  
24

1 signals "MIDCHIP" and "LASTCHIP" which are used for generating the  
2 bit rate clock.

3 Fig. 10.0401 provides a circuit drawing showing construction details  
4 of a PN generator shift register cell "pngsreg" included in the PN  
5 processor.

6 Figs. 10.0402AA-CB provide a circuit drawing showing construction  
7 details of a PN generator shift register summer "pngssum" included in  
8 the PN generator shift register.

9 Fig. 10.05 is a circuit drawing showing construction details of a  
10 PN controller D type flip-flop "pnddff" included in the PN processor.

11 Figs. 10.06AA-DH provide a circuit drawing showing construction  
12 details of differential and PN encoder "dpenc" included in the PN  
13 processor. The differential and PN encoder includes circuitry shown on  
14 the left in Figs. 10.06AA-DH which performs differential encoding. The  
15 circuitry encodes data such that zeros in the incoming data cause the  
16 output to transition from either zero to one or one to zero, and ones  
17 in the incoming data cause the output not to transition. Other forms  
18 of differential encoding can be performed. For example, the circuitry  
19 can encode data such that ones in the incoming data cause the output  
20 to transition from either zero to one or one to zero, and zeros in the  
21 incoming data cause the output not to transition. A selection of one  
22 of these two forms of differential encoding is performed by placing a  
23 high or low signal on a selection line "DIFFSEL." Whether or not  
24 differential encoding takes place at all is also selectable. The



1 differential and PN encoder further includes circuitry shown on the right  
2 in Figs. 10.06AA-DH which PN encodes the data, if spread spectrum  
3 modulation is selected.

4 Figs. 10.07AA-CD provide a circuit drawing showing construction  
5 details of a PSK/FSK generator "fskgen" included in the PN processor.  
6 The PSK/FSK generator "fskgen" takes as its input a clock which runs  
7 at the chip rate (9.538 MHz in the illustrated embodiment). The  
8 PSK/FSK generator "fskgen" generates a tone for phase shift keying  
9 (e.g., 596 kHz in the illustrated embodiment). The PSK/FSK generator  
10 "fskgen" further includes circuitry shown at the bottom in Figs. 10.07AA-  
11 CD which switches phase according to the input data. In other words,  
12 this circuitry compliments ones to zeros, and zeros to ones according  
13 to input data. If PSK or FSK is not selected, data passes through the  
14 PSK/FSK generator unaltered.

15 Figs. 10.0701AA-AB provide a circuit drawing showing construction  
16 details of a FSK counter bit "fskcbt" included in the PSK/FSK  
17 generator.

18 Figs. 11AA-AB provide a circuit drawing of a battery I/O buffer  
19 "batalg" included in the integrated circuit 16. In one embodiment,  
20 battery voltage is compared to band gap voltage (produced by the band  
21 gap reference generator) using an op-amp. In one embodiment, the  
22 battery I/O buffer "batalg" is used to connect a voltage to the analog  
23 to digital converter; however, in the illustrated embodiment, this function  
24 is performed by a circuit "tsn." The circuit "tsn" includes an enable

1 line, and includes a resistor divider. When an enable signal is placed  
2 on the enable line, the resistor divider is tapped, and the output of the  
3 resistor divider goes to an op-amp for comparison with band gap  
4 voltage.

5 In order to detect a low battery voltage, circuitry is provided  
6 which defines what is a low voltage. The lowest possible value at  
7 which an indication is given that the battery voltage is low is the value  
8 at which the integrated circuit 16 begins to fail to operate properly.  
9 However, in a preferred embodiment, an extra margin is provided so  
10 that there is time to replace the battery or replace the device before  
11 the integrated circuit 16 fails. For example, in one embodiment, the  
12 margin is 0.1 Volts. The circuitry "tsn" is therefore set up with a  
13 voltage divider having a tap compared to the band gap voltage. The  
14 voltage divider has resistor values selected so that when battery voltage  
15 is at the margin (e.g. 0.1 Volts) above the lowest possible value, the  
16 tap in the voltage divider has a voltage slightly below the band gap  
17 voltage (e.g., 1.2 Volts).

18 Figs. 12AA-AB provide a circuit drawing of a digital I/O pad  
19 buffer "paddig" included in the integrated circuit 16. The digital I/O  
20 pad buffer is both an input and output buffer. The I/O pad buffer  
21 "paddig" has an input "DPAD" which is connected to a bond pad of  
22 the integrated circuit 16. Data entering the pad buffer "paddig" from  
23 the input "DPAD" passes through an ESD protection device "esd1" and  
24 then passes on to whatever circuit for which it is an input (there are

1 many such pad buffers "paddig" in the illustrated embodiment). Data  
2 to be output via the pad buffer "paddig" comes into the pad buffer  
3 "paddig" via a line "DOUT" along with an enable on line "ENABLE."  
4 The pad buffer "paddig" includes a static pull down device shown on  
5 the far right in Figs. 12AA-AB. The pad buffer "paddig" further  
6 includes n-channel and p-channel transistors shown in the right in Figs.  
7 12AA-AB proximate the static pulldown device. If an enable signal is  
8 present on line "ENABLE" and "DOUT" is high, the two p-channel  
9 devices will turn on and pull the output pad "DPAD" high. If  
10 "DOUT" is low, the two n-channel devices will turn on and pull the  
11 output pad "DPAD" low. The pad buffer "paddig" further includes  
12 circuitry providing for gradual pulling high or pulling low to reduce  
13 transient currents. This is because a user may connect the pad to  
14 drive a heavy load.

15 Fig. 13 provides a circuit drawing of a digital input pad buffer  
16 "padigin" included in the integrated circuit 16. Fig. 13 shows the input  
17 portion only of the pad buffer "paddig."

18 Fig. 14 provides a circuit drawing of an analog I/O pad buffer  
19 "padalg" included in the integrated circuit 16. In one embodiment, the  
20 analog I/O pad buffer is used to connect an external sensor to the  
21 analog to digital converter.  
22  
23  
24

## Details of RF Selectable Return Link

The return link configuration logic "rlconfig" provides for user customization of operation of the transmitter "tx." Various customizations are possible. For example, the transmitter "tx" is selectable as operating in a backscatter transmit mode, or an active transmit mode in response to a command from the interrogator 26. This is shown in Figs. 21 and 22. Fig. 21 is a simplified circuit schematic illustrating a transmitter "tx" switchable between an active mode and a backscatter mode, and employing separate antennas As1 and As2 for the active mode and the backscatter mode, respectively. If the active mode is selected, the micro controller connects the antenna As1 to transmit the output of the transmitter, using switch S1. If the backscatter mode is selected, the micro controller 34 connects the antenna As2 to transmit the output of the transmitter, using switch S2. In an alternative embodiment, shown in Fig. 22, the transmitter "tx" is still switchable between an active mode and a backscatter mode, but employs the same antenna 46 for both the active mode and the backscatter mode.

If the backscatter mode is selected, the interrogator 26 sends a continuous unmodulated RF signal while the transmitter "tx" transmits a response to a command from the interrogator 26. The clock recovered from the incoming message is used to derive a subcarrier for the transmitter "tx." In the illustrated embodiment, the subcarrier for the transmitter "tx" is a square wave subcarrier. The response to the

1 interrogator is modulated onto the square wave subcarrier by the  
2 device 12 using a selected modulation scheme. For example, the  
3 response can be modulated onto the subcarrier using Frequency Shift  
4 Keying (FSK), or Binary Phase Shift Keying (BPSK).

5 If the active transmit mode is selected, the transmitter 32 is  
6 selectable as using amplitude modulation, or bi-phase (Binary Phase Shift  
7 Keying) modulation. The transmitter 32 is selectable as using  
8 differential coding, and/or spread spectrum coding. There are various  
9 combinations of options that can be selected through the commands that  
10 are sent to the integrated circuit 16 by the interrogator 26. The  
11 transmitter 32 is selectable as using the thirty-one chip spread spectrum  
12 sequence, or a narrow band.

13 These options provide for a wide range of possible applications  
14 or uses for the integrated circuit 16, and provide for the possibility of  
15 using different schemes in an application for different purposes. For  
16 example, an active transmit can be selected for certain purposes, while  
17 a backscatter transmit can be selected for different purposes.

18 Figs. 15AA-BC provide a circuit drawing of return link  
19 configuration control logic "rlconfig." The return link configuration  
20 control logic "rlconfig" has inputs "TXSEL0," "TXSEL1," and "TXSEL2."  
21 The values on these inputs are defined by a radio frequency command  
22 sent by the interrogator. These inputs "TXSEL0," "TXSEL1," and  
23 "TXSEL2" are connected to the outputs of an output register "oreg"  
24 included in the processor. The return link configuration logic takes

each possible combination of inputs "TXSEL0," "TXSEL1," and "TXSEL2" (there are a total of  $2 \times 2 \times 2 = 8$  possible combinations) and asserts appropriate control signals to enable the desired return link configuration. The signals being controlled by the return link configuration control logic "rlconfig" are: "ENDIL" for enabling the data interleaver; "PNOFF" for selecting whether or not PN encoding is employed for data transmitted by the device 12; "DIFFSEL" for selecting which polarity of differential encoding is used for transmitted data; "DIFFON" for selecting whether or not differential encoding is employed for transmitted data; and "ENFSK" for selecting FSK (or PSK in an alternative embodiment) for transmitted data; "BSCAT" for enabling backscatter for transmitted data; and "ENABLEAM" enables amplitude modulation.

The integrated circuit 16 further includes a number of sensors, such as sensors "batalg," "tsn," and "mag," in the embodiments where an A/D converter is included in the analog processor "anlgproc." The sensor "batalg" is a battery voltage detector, the sensor "tsn" is a temperature sensor, and the sensor "mag" is a magnetic sensor. These sensors will be connected to the A/D converter in the analog processor "anlgproc" in one embodiment of the invention. In one embodiment, one or more of these sensors are not included or not used.

Using such sensors, the device 12 can monitor things such as its own battery voltage, its temperature and detect the presence of a magnetic field. There are various possible uses for information sensed

1 by such sensors. For example, events can be counted so that,  
2 depending on the user's application, the user can determine whether or  
3 how many times a certain item was exposed to temperature above or  
4 below a certain value (e.g., to determine likelihood of spoilage or  
5 damage). Alternatively, the user can determine whether or how many  
6 times a certain item was exposed to a magnetic field of a certain value  
7 (e.g., when passing a certain location).

8 Figs. 16AA-EH provide a circuit drawing showing construction  
9 details of the temperature sensor "tsn." The temperature sensor "tsn"  
10 was designed to put out a voltage that is linearly proportional to  
11 temperature. In the illustrated embodiment, the circuit "tsn" has been  
12 reconfigured for use as a low battery voltage detector.

13 Figs. 16.01AA-DI provide a circuit drawing showing construction  
14 details of an operational amplifier "opamp" included in the temperature  
15 sensor "tsn."

16 Figs. 17AA-BB provide a circuit drawing of a magnetic field  
17 sensor "mag." The magnetic field sensor senses magnetic fields.

18 Figs. 18AA-AB provide a circuit drawing showing a chip bypass  
19 capacitor "bypcap3." The capacitor "bypcap3" is a integrated circuit  
20 decoupling capacitor between Vdd and ground.

21 Fig. 19AA-EK provide a circuit drawing of a semiconductor  
22 integrated circuit in accordance with an alternative embodiment of the  
23 invention. The integrated circuit of Figs. 19AA-EK is similar to the  
24 integrated circuit shown in Figs. 6AA-EK, like components having like

1 component names, except that the integrated circuit of Figs. 19AA-EK  
2 has no ROM, and is intended to be connected to an external ROM.  
3 This is useful for test purposes.

4 Figs. 20AA-DF provide a circuit drawing of a data processor  
5 "dataproc\_t3" to be used in the integrated circuit of Fig. 19 in place  
6 of the data processor "dataproc." The data processor "dataproc\_t3" has  
7 an interface to external ROM.

8 Figs. 20.01AA-CB provide a circuit drawing of an interface  
9 "extrom" to an external ROM.

10 Figs. 20.0101AA-BB provide a circuit drawing of external ROM  
11 control logic "extromctl" included in the interface "extrom."

12 Fig. 20.0102 is a circuit drawing of an external ROM address  
13 interface "extromad" included in the interface "extrom."

14 Figs. 20.0103AA-AC provide a circuit drawing of a digital I/O pad  
15 buffer "paddigt3" included in the interface "extrom." The digital I/O  
16 pad buffer "paddigt3" is the pad driver for the external ROM.

17 Fig. 20.0104 is a circuit drawing of an external ROM databus  
18 interface "extromdb" included in the interface "extrom."

19 Figs. 6AA-EK also illustrate bonding pads "PAD AA," and "PAD  
20 A," "PAD B," "PAD C," "PAD D," "PAD E," "PAD F," "PAD G," "PAD  
21 H," "PAD I," "PAD J," "PAD K," "PAD L," "PAD M," "PAD N," "PAD  
22 O," "PAD P," "PAD Q," "PAD R," "PAD S," "PAD T," "PAD U," "PAD  
23 V," "PAD W," "PAD X," "PAD Y," and "PAD Z," which are provided  
24 around the edge of the die of integrated circuit 16. In the illustrated



embodiment, the integrated circuit 16 includes a standard 20 lead SOIC package; however, any appropriate integrated circuit package can be employed.

Connections to these pads are brought out of the package and are accessible to the user. In this way, the user can somewhat tailor the function of the integrated circuit 16 to their application. In one embodiment, however, the entire device 12 is encapsulated in a housing such as that shown in Fig. 3.

The pads P and Q are digital port data and clock pads, and work together to provide a serial input or output, or a digital connection outside the integrated circuit. For example, if desired, data can be transmitted to the integrated circuit 16 via radio frequency, and a response can be put out on the digital port data pad, or vice versa.

The pad R is a chip enable pad, and prevents wake up to look for an incoming radio frequency signal. There are some applications or uses where the user knows that there will be certain periods of time when no valid radio frequency signals will be presented to the integrated circuit 16. The user will want to prevent the integrated circuit 16 from leaving the sleep mode so that power can be saved, and the life of the battery 18 can be extended.

The pad S is a test mode pad for testing. When the integrated circuit 16 is powered on (i.e., when power is first applied), if that pad is held high then the micro controller 34 goes into a self-test mode. After the self-test, if the pad S is no longer held high, the integrated

1 circuit 16 goes to the sleep mode, and periodically awakens to look for  
2 valid radio frequency signals, as it normally would. This pad S is  
3 useful to the manufacturer of the integrated circuit 16, such as for  
4 testing prior to packaging the die of the integrated circuit 16 in the  
5 housing of the integrated circuit 16.

6 The pad T is a digital transmit pad, and the pad U is a digital  
7 transmit data pad. These pads are useful for testing. They allow the  
8 integrated circuit 16 to operate in its intended manner, except that, if  
9 the pad T is held high, data from the integrated circuit 16 is brought  
10 out as a digital signal on the pad U instead of being transmitted via  
11 radio frequency using transmitter "tx."

12 If the pad I is held high, data to the integrated circuit 16 is  
13 brought in as a digital signal on the pad H instead of being received  
14 via radio frequency using receiver "rx". Details of the logic associated  
15 with this function are included in the Fig. 8.01 in connection with lines  
16 "DIGRX" (associated with pad I) and "DIGRXDATA" (associated with  
17 pad H). This logic includes the NAND gates and invertors shown  
18 leading from the lines "DIGRX" and "DIGRXDATA" to a line "DataIn."

19 These pads T, U, I, and H provide for testing of most functions  
20 of the integrated circuit 16 without the need to use high frequency  
21 radio signals. High frequency radio signals may not always be  
22 convenient in a testing lab. The pads T and U do not provide for  
23 testing of some functions relating to radio frequency transmission, and  
24 the pads I and H do not provide for testing of some functions relating

1 to radio frequency reception (e.g., operation of the Schottky detector).  
2 These pads T, U, V, and H do provide for testing of the spread  
3 spectrum processing circuit 40, and for processing of protocol commands  
4 described in the appended microfiche. This allows everything but  
5 operation of radio frequency transmitter 32 and receiver 30 to be  
6 checked prior to proceeding with that radio frequency testing. It also  
7 provides a function for the user, in that the integrated circuit 16 does  
8 not necessarily need to be used as a radio frequency identification  
9 device. The integrated circuit 16 has a receiver, and a transmitter, and  
10 it can be used for various purposes, such as an actuator or beacon.  
11 If it is not necessary to have a radio transmission or reception of data,  
12 either one or both form of data can be passed directly through the  
13 pads in digital form.

14 Note that there are separate enables T and I associated with  
15 transmitting or receiving digital data. For example, if the digital  
16 transmit pad T is taken high, then the transmitter "tx" will not cause  
17 a radio frequency signal to travel to antenna 46 but instead outgoing  
18 responses will come out on the pad U. However, the receiver "rx" will  
19 operate normally unless the digital receive pad I is taken high.

20 The pad V is a TX clock pad, or transmit clock pad. Pad V  
21 was intended to be an external input that could be used for a clock  
22 for the transmitter 32 instead of the clock recovered from the incoming  
23 signal. In some applications, it may be necessary to have a clock that  
24 is more stable than the recovered clock, and the pad V provides a way

1 for the user to supply such a clock. For example, the user may  
2 connect a crystal oscillator, external to the integrated circuit 16, and  
3 that way achieve a very stable carrier frequency for the transmitter "tx."  
4 In the illustrated embodiment, pad V has been reconnected to provide  
5 a signal which can be used to activate an external, high performance  
6 radio.

7 The pads Y, Z, AA, A, and D are antenna pads for connecting  
8 the receiver 30 and transmitter 32 to the shared antenna 14 or the  
9 multiple antennas 44 and 46. In the preferred embodiment, circuitry  
10 that interfaces these pads is physically located on the die next to these  
11 pads. More particularly, the microwave outputs of the transmitter 32  
12 are arranged on the die so as to be next to (in close physical  
13 proximity to) the appropriate bond pads.

14 The pad B is a test RX or test receive pad, and the pad C is  
15 a test TX or test transmit pad. Because the integrated circuit 16 is  
16 usually in the sleep mode, but wakes up briefly to look for a valid  
17 incoming radio frequency signal, and then goes back to sleep, it can be  
18 difficult to test the receiver "rx" and the transmitter "tx." Therefore the  
19 pads B and C provide for forcing on the receiver "rx" and  
20 transmitter "tx," respectively, such as for testing. If a high signal is  
21 applied to the pad B, this forces the receiver "rx" to remain on.  
22 Similarly, if a high signal is applied to the pad C, this forces the  
23 transmitter "tx" to remain on.  
24

1 If the pad B is used to force the receiver on in order to  
2 exercise the circuitry, such as through clock recovery, an input radio  
3 frequency signal is required at the appropriate frequency (e.g., 2.45  
4 GHz) modulated with the spread spectrum code.

5 The pad E is a RX input or receive input pad. This pad is  
6 connected to a side of the Schottky detector where the base band  
7 signal is available. This pad is provided for test purposes and to allow  
8 the use of a high-performance Schottky diode external to the integrated  
9 circuit 16.

10 The pad G is a VSS A pad, or analog VSS pad. The pad G  
11 is a connection to a ground bus that only goes to the analog circuitry.

12 Other pads J, K, L, M, N, O, and W are voltage supply or  
13 voltage drain pads (Vss or Vdd).

#### 14 15 Protocol

16 A description of a protocol which can be employed by the  
17 device 12 for the commands, replies, and status information is contained  
18 in a manual titled "Micron RFID Systems Developer's Guide." This  
19 manual relates to a device for use with an "AMBIT" (TM) brand  
20 tracking system as well as to the device 12. Also relevant is U.S.  
21 Patent No. 5,500,650 to Snodgrass et al., titled "Data Communication  
22 Method Using Identification Protocol," incorporated by reference.

23 Examples of commands that can be sent from the interrogator 26  
24 to the device 12 are as follow:

### Identify

An Identify function is used when attempting to determine the identification of one or more of the devices 12. Each device 12 has its own identification number TagId. It is possible that the interrogator will receive a garbled reply if more than one tag responds with a reply. If replies from multiple tags are received, an arbitration scheme, discussed below, is used to isolate a single device 12.

### ReadAnalogPort

In one embodiment, a ReadAnalogPort function is provided which returns the voltage (eight-bit value) of a selected analog port on a device 12.

### ReadDigitalPort

A ReadDigitalPort function returns data read from a serial port of a device 12.

### ReadTagMemory

A ReadTagMemory function returns data from a user accessible portion of memory included in a device 12.

### ReadTagStatus

A ReadTagStatus function returns system information about a specified device 12. For example, in response to this command, the

1 device 12 will transmit a confirmation of its TagId, a tag revision  
2 number, the low battery status bit, and other information.

#### 3 4 SetAlarmMode

5 In one embodiment, a SetAlarmMode function is provided which  
6 is used to determine if a set point has been exceeded on an analog  
7 port of the device 12 (e.g., if a sensor senses a condition exceeding a  
8 predetermined threshold). There are three alarm modes:  
9 SET\_HIGH\_BAND\_ON\_ALARM, SET\_LOW\_BAND\_ON\_ALARM, and  
10 SET\_STATUS\_REG\_ON\_ALARM.

11 The SET\_HIGH\_BAND\_ON\_ALARM mode sets a device 12 to a  
12 low data band, and clears a bit in the device's status register indicative  
13 of an alarm threshold being exceeded. When a set point (threshold)  
14 is violated, the device 12 will switch from the low data band to a high  
15 data band.

16 The SET\_LOW\_BAND\_ON\_ALARM mode sets a device 12 to a  
17 high data band, and clears a bit in the device's status register indicative  
18 of an alarm threshold being exceeded. When a set point (threshold)  
19 is violated, the device 12 will switch from the high data band to the  
20 low data band.

21 The SET\_STATUS\_REG\_ON\_ALARM mode does not change data  
22 bands, but will result in a bit ALARM\_THRESHOLD\_EXCEEDED in  
23 the status register being set if the set point is violated.  
24

### SetMemoryPartition

A SetMemoryPartition function defines (initializes) a block of user memory in a device 12 for memory partition. After being initialized, a partition may be used to store data using a function WriteTagMemory. Data may be read from the partition using a function ReadTagMemory. The number of partitions available on a device 12 can be determined using the ReadTagStatus function.

### WriteAccessId

A WriteAccessId function is used to update an access identification AccessId for one of the memory partitions.

### WriteDigitalPort

A WriteDigitalPort function is used to write data to the synchronous serial port of a device 12.

### WriteTagId

A WriteTagId function is used to update the TagId of a device 12.

### WriteTagMemory

A WriteTagMemory function is used to write to the user memory space UserMemory of a device 12.



### WriteTagsRegs

A WriteTagsRegs function is used to update selected or all registers of a device 12 including registers TagControlReg, LswTagId, TagStoredInterrId, TimedLockoutCounter, and DormantCounter for a range of RandomValueIds. This command can be used, for example, to disable a device 12. If desired, the transmitter of a device 12 can be disabled while the receiver of that device 12 is left functional. This is accomplished using bits KILL\_TAG\_0 and KILL\_TAG\_1 in a register TagControlReg.

### WriteTagRegsRandIdRange and WriteTagRegsTagIdRange

WriteTagRegsRandIdRange and WriteTagRegsTagIdRange functions are used to update registers of a group of devices 12. The WriteTagRegsTagIdRange function updates selected or all registers, including registers TagControlReg, LswTagId, TagStoredInterrid, TimedLockoutCounter, and DormantCounter, for a range of TagIds.

Examples of interrogator commands are as follows:

### GetCrntAntenna

A GetCrntAntenna function returns the current antenna set used to communicate with a device 12.

### GetCrntRetries

A GetCrntRetries function returns the number of times a command was re-transmitted during the last tag-specific command.

### GetInterrStats

A GetInterrStats function returns record-keeping parameters if the interrogator performs this function.

### GetReplyStats

A GetReplyStats function returns values that are specific to the last tag-specific reply if the interrogator processes this information.

### SetInterrRegs

A SetInterrRegs function is used to set various communication parameters on an interrogator. Not all of the parameters are used on all interrogators.

### SetInterrTest

A SetInterrTest function is used during testing. This function should not be called in normal operation.

1       SetTimeouts

2       A SetTimeouts function is used to set the system watchdog timers.

3  
4       A convenience command is described as follows:

5  
6       IdentifyAll

7       An IdentifyAll function returns the number of devices 12 found  
8       within the system's communication range. The IdentifyAll reply  
9       parameters include the TagId and RandomValueId for each device 12  
10      that is identified.

11  
12      The sequence of steps performed by a device 12 upon receipt of  
13      an Identify command from an interrogator will now be provided,  
14      reference being made to Figs. 55-57.

15      Fig. 55 illustrates top level steps, held in ROM, performed by the  
16      data processor of the device 12 upon wake up (upon leaving a sleep  
17      mode 500) for any reason. The sleep mode is described above.

18      At step 502, a determination is made as to whether the device  
19      12 is in a test mode. Test mode is enabled by holding a special pin  
20      high at power up time. If so, the data processor proceeds to step 504;  
21      if not, the data processor proceeds to step 506.

22      At step 504, a test routine is performed. The current test  
23      routine checks the Rom, RAM, processor registers, and the timed  
24

1 lockout timer. After performing step 504, the data processor proceeds  
2 to step 500 (the device 12 returns to the sleep mode).

3 At step 506, a determination is made as to whether the device  
4 12 is being powered up according to the status of a signal provided by  
5 a power up detector circuit. If so, the data processor proceeds to step  
6 508; if not, the data processor proceeds to step 510.

7 At step 508, a power up routine is performed which initializes the  
8 wakeup timer, sets up the control register, and clears the RAM. After  
9 performing step 508, the data processor proceeds to step 500 (the  
10 device 12 returns to the sleep mode).

11 At step 510, a determination is made as to whether a protocol  
12 request has been issued. If so, the data processor proceeds to step  
13 512; if not, the data processor proceeds to step 514.

14 At step 512, the data processor executes a command processing  
15 routine. The command processing routine is described in greater detail  
16 below, in connection with Figs. 56A-B. After performing step 512, the  
17 data processor proceeds to step 500 (the device 12 returns to the sleep  
18 mode).

19 At step 514, a determination is made as to whether an alarm  
20 timer request has been issued. This occurs once each minute. If so,  
21 the data processor proceeds to step 516; if not, the data processor  
22 proceeds to step 500 (the device 12 returns to the sleep mode).

23 At step 516, the data processor performs an alarm timer routine,  
24 which in one embodiment allows a selected analog input to be

1 compared against a threshold. The results of the comparison can be  
2 used to set a bit and optionally cause the chip to change data bands.

3 The command processing routine 512 is illustrated in greater detail  
4 in Fig. 56.

5 At step 518, high signals are placed on lines SIOENABLE and  
6 RFENABLE to enable the serial input output block "sio" and to enable  
7 radio frequency communications. After performing step 518, the data  
8 processor proceeds to step 520.

9 At step 520, a determination is made as to whether RFDET is  
10 high indicating that an RF signal is still present at the receiver input.  
11 If so, the data processor proceeds to step 522; if not, the data  
12 processor proceeds to step 524.

13 At step 524, the command processing routine is aborted, and the  
14 device 12 returns to the sleep mode.

15 Steps 522, 526, 528, and 532 are used to determine whether a  
16 first byte of a command is received within a predetermined amount of  
17 time after the chip wakes up and successfully acquires the clock signal  
18 from the incoming preamble.

19 At step 522, a counter is initialized according to the wakeup  
20 interval selected. After performing step 522, the data processor  
21 proceeds to step 526.

22 At step 526, a determination is made as to whether the counter  
23 has counted down to zero. If so, the data processor proceeds to step  
24 524; if not, the processor proceeds to step 528.

1 At step 528, a determination is made as to whether the first byte  
2 of a valid incoming radio frequency signal has been detected. If so,  
3 the processor proceeds to step 530; if not, the processor proceeds to  
4 step 532.

5 At step 532, the counter is decremented. After performing step  
6 532, the data processor proceeds to step 526.

7 At step 530, the data processor reads in a command string from  
8 the serial input output block "sio" and stores the command string in  
9 random access memory. The serial input output block "sio" controls  
10 transfer of an incoming radio frequency message from the receiver to  
11 the data processor. After performing step 530, the data processor  
12 proceeds to step 534.

13 At step 534, the high signals on lines RFENABLE and  
14 SIOENABLE are cleared. After performing step 534, the data  
15 processor proceeds to step 536.

16 At step 536, the receiver is turned off in order to conserve  
17 power. After performing step 536, the data processor proceeds to step  
18 538.

19 At step 538, a determination is made using CRC as to whether  
20 transmission occurred without errors. If so, the data processor proceeds  
21 to step 540; if not, the data processor proceeds to step 524. CRC is  
22 cyclic redundancy checking, a technique known in the art used to detect  
23 errors in transmission of data by the affirmation of error codes by both  
24

1 the sending and receiving devices. In one embodiment, a check sum  
2 is used in place of a CRC.

3 At step 540, a determination is made as to whether the device  
4 12 was killed by a previous command. If so, the data processor  
5 proceeds to step 542; if not, the data processor proceeds to step 544.

6 At step 542, a determination is made as to whether the received  
7 command is a WriteTagRegs command which can reset the kill bits in  
8 the control register. If so, the data processor proceeds to step 544;  
9 if not, the data processor proceeds to step 548, which is identical to  
10 step 524 on the previous page of the diagram.

11 At step 544, a determination is made as to whether a valid  
12 command token exists for the received command. If so, the data  
13 processor proceeds to step 546; if not, the data processor proceeds to  
14 step 548.

15 At step 546, a determination is made as to whether variables  
16 TagID and InterrID transmitted to the device 12 correctly correspond  
17 to the identification number for the particular device 12 and the  
18 identification number for the interrogator with which the particular  
19 device 12 is to correspond. If so, the data processor proceeds to step  
20 550; if not, the data processor proceeds to step 548.

21 At step 548, the command processing routine is aborted, and the  
22 device 12 returns to the sleep mode.

23 At step 550, the data processor jumps to code for the specific  
24 command that was received by radio frequency. If the command is an

1 Identify command, the data processor will jump to step 552, which is  
2 the start of an Identify command routine.

3 The Identify command routine is illustrated in Figs. 57A-B.

4 At step 554, a determination is made as to whether a timed  
5 lockout has been set by a previously received command. If so, the  
6 data processor proceeds to step 556; if not, the data processor proceeds  
7 to step 558.

8 At step 556, the Identify command routine is aborted, and the  
9 device 12 returns to the sleep mode.

10 At step 558, a determination is made as to whether a variable  
11 "InterrID" transmitted to the device 12 correctly corresponds to the  
12 identification number for the interrogator with which the particular  
13 device 12 is to correspond. If so, the data processor proceeds to step  
14 560; if not, the data processor proceeds to step 556.

15 At step 560, Arbitration Lockout is cleared if this is requested.  
16 After performing step 560, the data processor proceeds to step 562.

17 At step 562, a new random number is obtained if this is  
18 requested. After performing step 562, the data processor proceeds to  
19 step 564.

20 At step 564, arbitration parameters are checked. After performing  
21 step 564, the data processor proceeds to step 566.

22 At step 566, a determination is made as to whether the particular  
23 device 12 should respond. If so, the data processor proceeds to step  
24 568; if not, the data processor proceeds to step 556.





1 At step 580, the data processor sends a reply to the Identify  
2 command to the interrogator via radio frequency. After performing step  
3 580, the data processor proceeds to step 582.

4 At step 582, the high signals on lines RFENABLE and  
5 SIOENABLE are cleared. After performing step 582, the data  
6 processor proceeds to step 584.

7 At step 584, transmit mode is cleared. After performing step  
8 584, the data processor proceeds to step 586.

9 At step 586, the processor pulses the Protocol Request  
10 Acknowledge signal which terminates the wakeup condition that initiated  
11 this entire routine. After performing step 586, the data processor  
12 proceeds to step 588.

13 At step 588, the data processor returns certain control register  
14 bits to their proper states in preparation for sleep mode.

15 The processor then proceeds to step 500 and returns to sleep  
16 mode.

17 The sequence of steps performed by an interrogator to issue an  
18 Identify command will now be provided, reference being made to Figs.  
19 58-60.

20 Fig. 58 illustrates steps performed by a host processor of the  
21 interrogator upon initialization. Initialization is started in step 600 by  
22 calling a function.

23 At step 602, a determination is made as to whether an attempt  
24 is being made to open more than a maximum number of interrogators.

1 If so, the host processor proceeds to step 604; if not, the host  
2 processor proceeds to step 606.

3 At step 604, an appropriate error message is returned by setting  
4 the parameter RFID ErrorNum to the appropriate value, and a null  
5 value is returned to the calling function.

6 At step 606, interrogator parameters are initialized. This includes  
7 initializing timeout values, interrogator types and ports. After  
8 performing step 606, the host processor proceeds to step 608.

9 At step 608, a determination is made as to whether a valid  
10 interrogator IO port has been selected. If so, the host processor  
11 proceeds to step 612; if not, the host processor proceeds to step 610.

12 At step 610, an appropriate error message is returned. The  
13 parameter RFID ErrorNum is set to the appropriate value and a null  
14 is returned to the calling function.

15 At step 612, function addresses are assigned. This includes the  
16 function to compute CRCs or checksums and the input and output  
17 routines. After performing step 612, the host processor proceeds to  
18 step 614.

19 At step 614, default communication values are assigned. This  
20 includes default selections for diversity and communication retries. After  
21 performing step 614, the host processor proceeds to step 616.

22 At step 616, communication hardware is reset. This initializes the  
23 interrogator into a known state by resetting the hardware and clearing  
24

1 the I/O FIFO's. After performing step 616, the host processor proceeds  
2 to step 618.

3 At step 618, a frequency synthesizer is initialized. This function  
4 programs the frequency synthesizer to the desired frequency. After  
5 performing step 618, the host processor proceeds to step 620.

6 At step 620, a determination is made as to whether the frequency  
7 synthesizer is programmed properly. This function is used to abort the  
8 initialization process if the frequency synthesizer cannot be programmed,  
9 thereby preventing subsequent communications to occur on inappropriate  
10 frequencies. If so, the host processor proceeds to step 622; if not, the  
11 host processor proceeds to step 624.

12 At step 622, an host memory pointer is returned that points to  
13 a structure that contains the initialized parameters. After performing  
14 step 622, program control is returned to the Host Application Code.

15 At step 624, an appropriate error message is returned in the  
16 RFID ErrorNum parameter and a null is returned to the calling  
17 function.

18 Fig. 59 illustrates an example of a software application, starting  
19 at step 630, that calls the Identify function and causes the interrogator  
20 to transmit an Identify command via radio frequency.

21 At step 632, the function shown and described above in  
22 connection with Fig. 58 is called. After a successful call to the open  
23 functions (step 632) the host computer proceeds to step 634.  
24

1 At step 634, a determination is made as to whether the function  
2 shown and described in connection with Fig. 58 was successfully opened.  
3 If so, the system proceeds to step 638; if not, the system proceeds to  
4 step 636.

5 At step 636, the host processor exits the application (or takes  
6 whatever steps are appropriate within the intended application).

7 At step 637, the parameters are initialized for an Identify  
8 Command.

9 At step 638, an Identify function (described below in connection  
10 with Fig. 60) is called. After performing step 638, the host library  
11 function proceeds to step 640.

12 At step 640, a determination is made as to whether a good reply  
13 was received from the device 12. If so, the host computer proceeds  
14 to step 642; if not, the host processor proceeds to step 644.

15 At step 642, reply parameters received from the device 12 are  
16 printed, displayed, or otherwise used or processed. After performing  
17 step 642, the host computer proceeds to step 646 where the application  
18 returns results and ends.

19 At step 644, the host processor exits the application or takes  
20 whatever steps are appropriate for a given application.

21 Fig. 60 illustrates the sequence of steps performed by the host  
22 library function at the starting at step 650, when an Identify command  
23 is issued to the device 12.  
24



At step 670, the reply packet is read from the reply FIFO. After performing step 670, the library routine proceeds to step 672.

At step 672, the reply packet is parsed into separate parameter buffers. After performing step 672, the host library returns program control to the host application (step 674), where processing for the Identify command terminates and the host application software continues.

#### Details of Arbitration

The arbitration of multiple interrogators per device 12 is a detection method based upon each interrogator using a unique interrogator ID (InterrId). The InterrId is sent to a device 12 in a command. The device 12 also stores an interrogator ID TagStoredInterrId. The TagStoredInterrId is only updated by a WriteTagRegsXXX command. A RcvdInterrId is included in replies from a device 12. If a TagStoredInterrId does not match the RcvdInterrId then the tag will not respond with a reply.

The arbitration of more than one tag per interrogator 26 is accomplished by using an ArbitrationValue and an ArbitrationMask during an Identify command. Contained within each device 12 is a random value ID (RandomValueld) and an arbitration lockout (IDENTIFY\_LOCKOUT) bit. The RandomValueld is set to a "random" binary number upon command by an interrogator. It may also be set by an Identify command setting a SELECT\_RANDOM\_VALUE bit in SubCmnd.

1 The following examples use a 1-byte ArbitrationValue for  
2 simplicity. If an interrogator 26 transmits an Identify command with its  
3 ArbitrationMask set to 0000 0000 (binary), all devices 12 in the  
4 receiving range will respond. If there is only one device 12,  
5 communications may proceed between the interrogator 26 and device 12.  
6 If there are multiple devices 12 responding, the interrogator 26 will  
7 detect a collision and will start the arbitration sequence. To start the  
8 arbitration sequence among multiple tags, the interrogator 26 instructs  
9 the tags to clear their IDENTIFY\_LOCKOUT bit and (possibly)  
10 re-randomize their RandomValueId values. The ArbitrationValue 0000  
11 0000 and ArbitrationMask 0000 0001 are then transmitted to all  
12 devices 12 in range. The devices 12 perform a logical ANDing  
13 (masking) of the ArbitrationMask and the RandomValueId. If the result  
14 matches the ArbitrationValue sent by the interrogator 26, the device or  
15 devices 12 will reply to the Identify command. If not, the interrogator  
16 26 will increment the ArbitrationValue to 0000 0001 and try again.

17 The interrogator 26 then checks each of the possible binary  
18 numbers (0000 0000 and 0000 0001 in this case) in the expanded mask  
19 (0000 0001) for a response by a device 12. If a single device 12  
20 responds to one of these values, the interrogator 26 will reply by  
21 commanding it to set its lockout bit. If any collisions are detected at  
22 this mask level, the mask would be widened again by one bit, and so  
23 on through the eight bit wide mask (256 numbers). If no collisions are  
24 detected for a particular ArbitrationValue and ArbitrationMask



1 combination, the TagId returned in the reply is used for direct  
2 communication with that particular device 12. During the arbitration  
3 sequence with up to about one hundred devices 12, the mask will  
4 eventually grow large enough such that all devices 12 can respond  
5 without collision. After the mask widens to four or five bits, more  
6 devices 12 have unique random numbers and single tag replies are  
7 received. Thus with each expansion of the ArbitrationMask, there are  
8 fewer and fewer tags left to Identify.

9 With a large number of tags in range, it is possible that several  
10 devices 12 will choose the same value for their RandomValueId. In  
11 this case, the complete mask will be used. Collisions will still occur  
12 and the remaining tags will be instructed to select a new Random  
13 ValueId. If an application dictates, for example, that one hundred tags  
14 will usually be present in range of the interrogator 26, it would be  
15 advantageous to start with the mask set to eight bit wide (11111111)  
16 and count up through 256 instead of starting with the mask set at 0000  
17 0000, followed by 0000 0001, 0000 0011, etc. Other arbitration schemes  
18 can be implemented by the user.

### 20 Applications

21 There are a large number of possible applications for devices such  
22 as the device 12. Because the device 12 includes an active  
23 transponder, instead of a transponder which relies on magnetic coupling  
24 for power, the device 12 has a much greater range.

1 One application for devices 12 is inventory control to determine  
2 the presence of particular items within a large lot of products.

3 Another application for devices 12 is electronic article surveillance  
4 (EAS). The devices 12 can be attached to retail items in a store  
5 having an interrogator 26 at the exits, for detection of unauthorized  
6 removal of retail items. The merchant can deactivate or remove  
7 devices 12 from retail items for which proper payment has been made.

8 Another application for devices 12 is to track migration of  
9 animals.

10 Another application for devices 12 is to counteract terrorism by  
11 monitoring luggage entering a plane to ensure that each item of luggage  
12 that enters the plane is owned by a passenger who actually boards the  
13 plane. The devices 12 can also be used to monitor luggage to locate  
14 lost luggage.

15 The device 12 can be use to track packages, such as courier  
16 packages.

17 The device 12 can be used to track hazardous chemicals or waste  
18 to ensure that it safely reaches a proper disposal site.

19 The device 12 can be used for security purposes, to track  
20 personnel within a building. The device 12 can also be used for access  
21 control.

22 The device 12 can be used to monitor and manage freight transit.  
23 For example, interrogators 26 can be placed at the entrance and exit  
24

1 of a terminal (e.g., a rail or truck terminal), to monitor incoming and  
2 outgoing shipments of vehicles bearing the devices 12.

3 The device 12 can be used to impede car theft. A European  
4 anti-theft directive (74/61/EEC) provides that all new car models sold  
5 after January 1997 must be fitted with electronic immobilizers and  
6 approved alarm systems. The devices 12 can be provided on keychains  
7 or within car keys, and interrogators 26 placed in cars, so that the  
8 vehicle will be inoperable unless the specified device 12 for a specific  
9 car is used. The interrogator 26 can control the door locks of a car,  
10 or the ignition of the car, or both. Because the device 12 includes  
11 memory, the interrogator 26 in the car can periodically automatically  
12 change values in the device 12 (like changing a password).

13 Devices 12 can be placed in cars and used in connection with  
14 electronic toll collections systems. Because the devices 12 can be used  
15 to identify the respective cars in which they are placed, interrogators  
16 26 in toll plazas can charge appropriate accounts based on which cars  
17 have passed the toll plaza.

18 Devices 12 can be placed in cars and used in connection with  
19 parking systems. Because the devices 12 can be used to identify the  
20 respective cars in which they are placed, interrogators 26 in parking  
21 areas can determine when a vehicle arrives and leaves a parking area.

22 The devices 12 can be used for inventory control of rental  
23 equipment.  
24

1 The devices 12 can be used where bar code labels will not  
2 properly work because of harsh environmental conditions (e.g., grease,  
3 dirt, paint).

4 In compliance with the statute, the invention has been described  
5 in language more or less specific as to structural and methodical  
6 features. It is to be understood, however, that the invention is not  
7 limited to the specific features shown and described, since the means  
8 herein disclosed comprise preferred forms of putting the invention into  
9 effect. The invention is, therefore, claimed in any of its forms or  
10 modifications within the proper scope of the appended claims  
11 appropriately interpreted in accordance with the doctrine of equivalents.  
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